AN11060

TEA172X 5 W to 11 W Power Supply/USB charger

Rev. 1 — 1 May 2012 Application note

Document information

Info	Content
Keywords	Ultra-low standby power, constant output voltage, constant output current, primary sensing, integrated high-voltage switch, integrated high-voltage start-up, USB charger, standby supply, 5 W to 11 W supply.
Abstract	The TEA172X are primary sensing controllers for power supplies up to 5 W or 11 W (depending on version) with an integrated high-voltage switch. No-load power is as low as 10 mW (depending on version) and they surpass the Energy Star 5 level requirement (30 mW). When the maximum output power is exceeded, the IC changes from constant voltage mode to constant current mode, which is ideally suited for battery charging.

Revision history

Rev	Date	Description
v.1	20120501	first issue

Contact information

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1. Introduction

The TEA172X family comprise a flyback controller with primary sensing and integrated high-voltage switch. An advanced burst mode and integrated high-voltage start-up circuit ensure a low no-load power consumption, depending on the version down to 10 mW.

When the maximum output power is reached, the constant output voltage control changes to a constant output current control for use as a charger. Versions are available for maximum output power of 5 W or 11 W.

The device is packaged in a space saving SO7 package with high-voltage spacer.

All values mentioned in this application note are typical values. The minimum and maximum and spread figures can be found in the TEA172X data sheet.

2. Scope

This application note describes the functionality, the control functions and the basic dimensioning of the circuit components of the TEA172X low-power adapter. Detailed transformer calculation is available in a separate calculation sheet.

3. TEA172X low-power adapter

The TEA172X features enable power engineers to design reliable, cost-effective and efficient adapter supplies with low no-load power consumption. These features result in the TEA172X needing a minimum number of external components.

3.1 Key features

- Flyback controller with integrated 700 V MOSFET
- Available maximum output power of 5 W or 11 W
- No-load power consumption down to 10 mW at 5 W output power depending on the version
- Primary sensed output voltage control, eliminating optocoupler for lower overall system costs.
- High average efficiency above 75 % over the entire load range thanks to advanced control modes.
- USB 1.1 and 1.2 compliant for mobile phone chargers
- Available in SO7 package with high-voltage spacer

3.1.1 Applications

- Mobile communications
  - Mobile or smart phone charger
  - Tablet PC charger

- Home appliances
  - Washing and drying machines
  - Refrigerators and freezers
  - Dish washers
  - Induction cookers
  - Air conditioners
- Computing and consumer
  - E-readers
  - Portable audio/video equipment
  - Set-top boxes
  - PC peripherals
- Industrial and residential
  - Smart metering
  - Lighting
  - Home and building automation
  - Heating, Ventilation, Air Conditioning (HVAC) equipment
  - Industrial automation and control

3.2 Basic application schematic

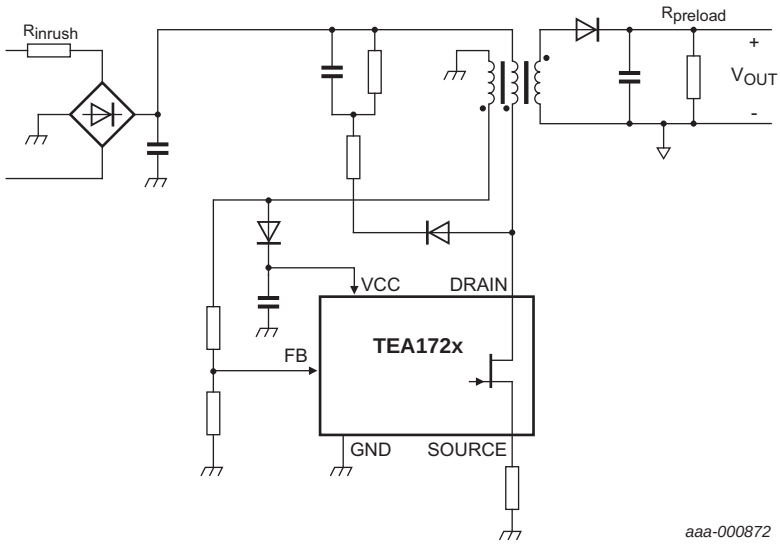


Fig 1. Basic application schematic

4. Pin description

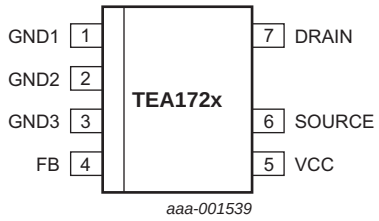


Fig 2. Pinning diagram SO7 TEA172X

Table 1. Pinning description

Pin	Name	Description
1	GND1	Ground connection from driver and control part. Pins GND1 and GND3 are thermally connected to the MOSFET and must be connected to a copper plane for efficient cooling.
2	GND2	
3	GND3	
4	FB	Feedback input. Senses the voltage on the auxiliary winding via a resistive divider during the secondary stroke. The sense voltage represents the voltage on the output winding At constant output voltage, the sensed voltage is regulated at 2.5 V. When the sensed voltage drops below 2.5 V, the regulation changes to Constant Current (CC) mode. The OverVoltage Protection (OVP) level is 3.2 V Demagnetization detection guarantees discontinuous operation. It checks that the voltage of the auxiliary winding drops below 50 mV after the secondary stroke.
5	VCC	Supply voltage. At start-up, an internal current source charges the capacitor until $V_{CC(startup)}$. $V_{CC(startup)}$ level is around 17 V. The device starts switching and the auxiliary winding takes over the supply. The $V_{CC(stop)}$ level on the VCC pin is 8.5 V.
6	SOURCE	SOURCE connection of the internal MOSFET. The current through the MOSFET is monitored using a resistor from the SOURCE pin to ground. The peak level in burst mode is around 120 mV. The peak level in other modes varies between 120 mV and 600 mV. (Exact values depend on the dV/dt value of the SOURCE pin.
7	DRAIN	DRAIN connection of the internal MOSFET. The breakdown voltage is 700 V. The high-voltage start-up current source is connected to the DRAIN pin.

5. System description

5.1 Introduction

Throughout this section, refer to the basic application schematic, Figure 1

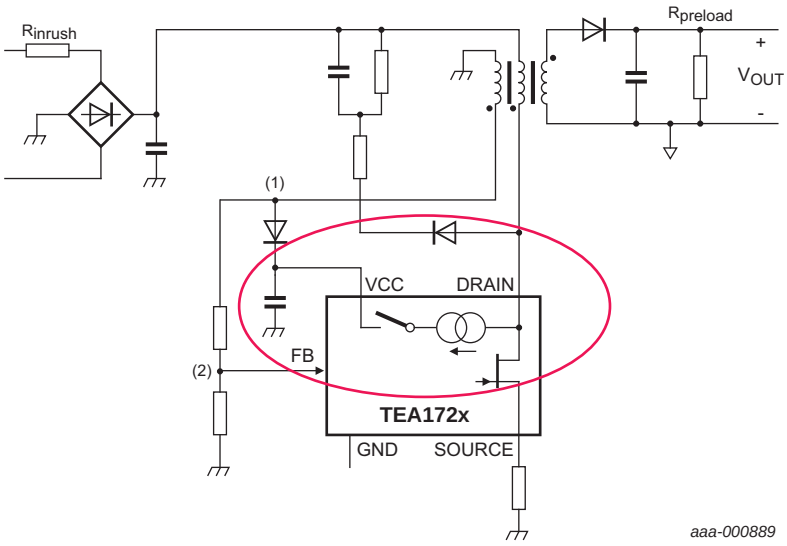
5.2 Supply

At start-up, an internal current source, connected to the DRAIN charges the capacitor connected to the VCC pin see Figure 3.

When the voltage level reaches 17 V ($V_{CC(startup)}$), the internal current source is switched off and the IC starts switching. The IC now runs using the charge on the capacitor connected to the VCC pin.

When the internal MOSFET starts switching, the voltage, generated at the auxiliary supply winding of the transformer provides the supply, see Figure 4. Under some circumstances, the IC does not start switching (due to protection) or the auxiliary winding does not provide the supply voltage. The result is, the capacitor VCC pin voltage drops to 8.5 V ($V_{CC(stop)}$), and the internal current source is enabled. The internal current source now charges the capacitor up to 17 V ($V_{CC(startup)}$). The sequence is repeated, see Figure 5

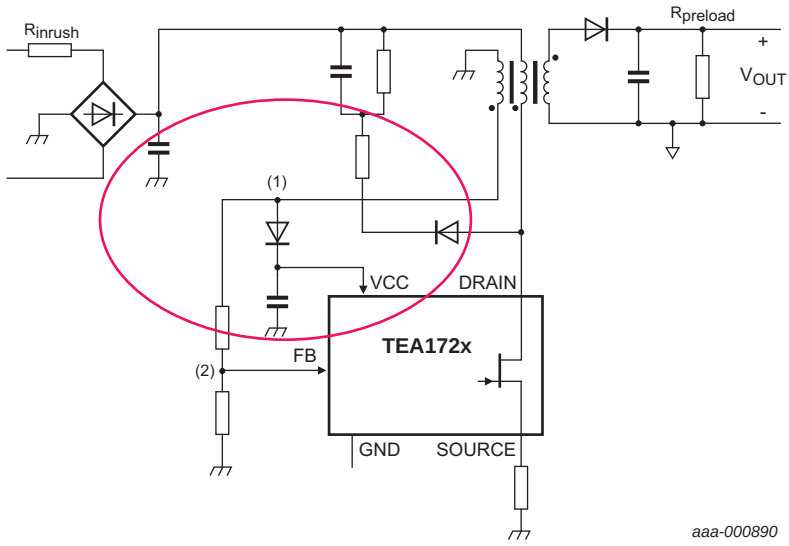
It is possible to supply the IC externally, however the supply voltage must be above 17 V ($V_{CC(startup)}$) with some margin to guarantee start-up. The rise time of the external supply voltage must be below 0.1 V/μs. If steeper, use a filter of for example, a 220 Ω series resistor and a 1 μF decoupling capacitor on the VCC pin. The example used is based upon a 20 V external supply.



(1) Auxiliary winding also provides VCC

(2) Primary sensing via auxiliary winding

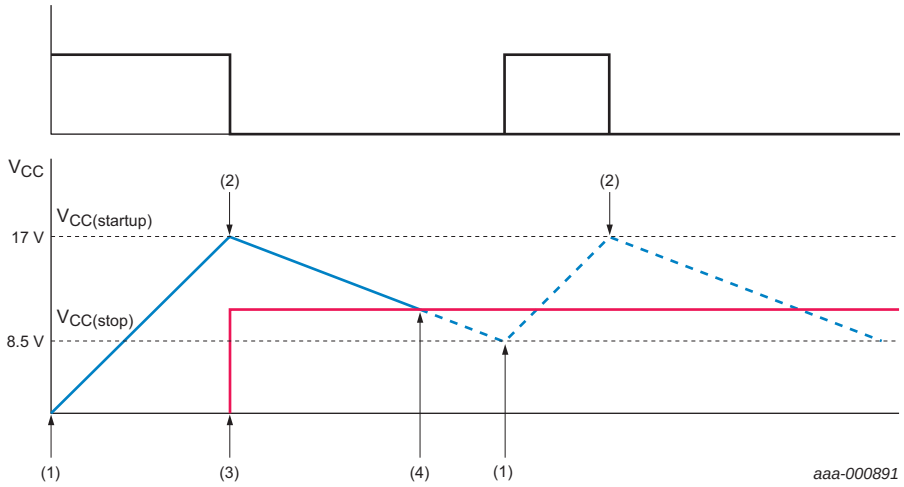
Fig 3. Charging the VCC capacitor



(1) Auxiliary winding also provides VCC

(2) Primary sensing via auxiliary winding

Fig 4. Rectified voltage of the auxiliary winding takes over the VCC supply



(1) HV current source on

(2) HV current source off

(3) Switching start, V_{AUX} builds up

(4) V_{AUX} takes over VCC

Fig 5. Voltage on the VCC pin

5.3 Operating modes

From no-load to maximum load and in CC mode, the TEA172X uses different operating modes as follows.

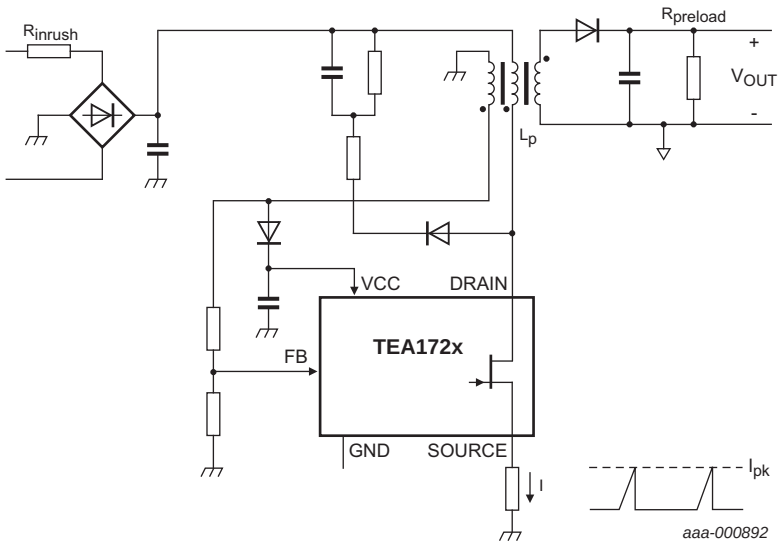


Fig 6. Basic circuit and relevant parameters

The regulation of a flyback converter is based upon regulating the transferred energy according to Equation 1.

$$P_o = 0.5 \times L_p \times I_{pk}^{2} \times f_{sw} \times \eta \quad (1)$$

Where:

- P_o = Output power
- L_p = Primary inductance of the transformer
- I_{pk} = The peak value of the primary current at switch-off from the MOSFET
- f_{sw} = Switching frequency
- η = Efficiency convertor

The output power is equal to the energy, stored per stroke, times the number of strokes per second times the efficiency. Though not accurate, the basic formula is enough to understand the control modes.

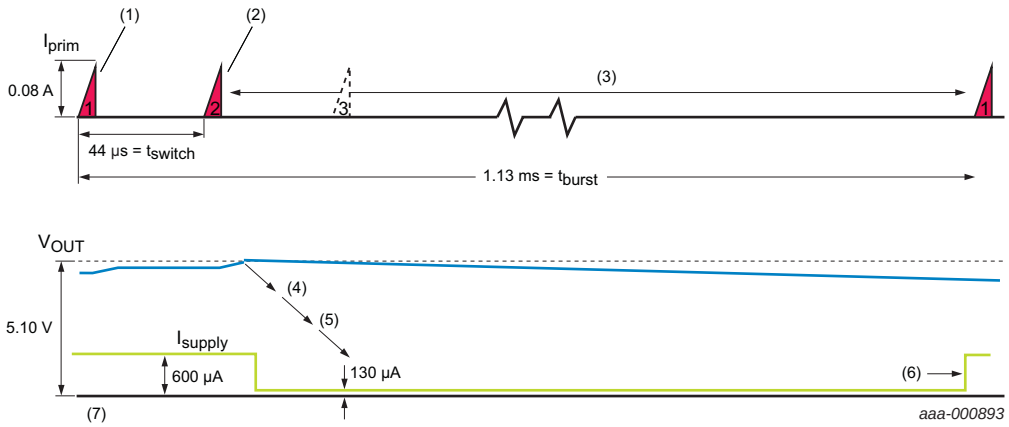
The different operating modes include:

- Constant Voltage Burst mode (CVB) regulation control
- Constant Voltage peak Current mode (CVC) regulation control
- Constant Voltage Frequency mode (CVF) regulation control
- Constant Current Frequency mode (CCF) regulation control
- Constant Current peak Current mode (CCC) regulation control

5.3.1 Burst mode

Figure 7 shows burst mode with energy saving.

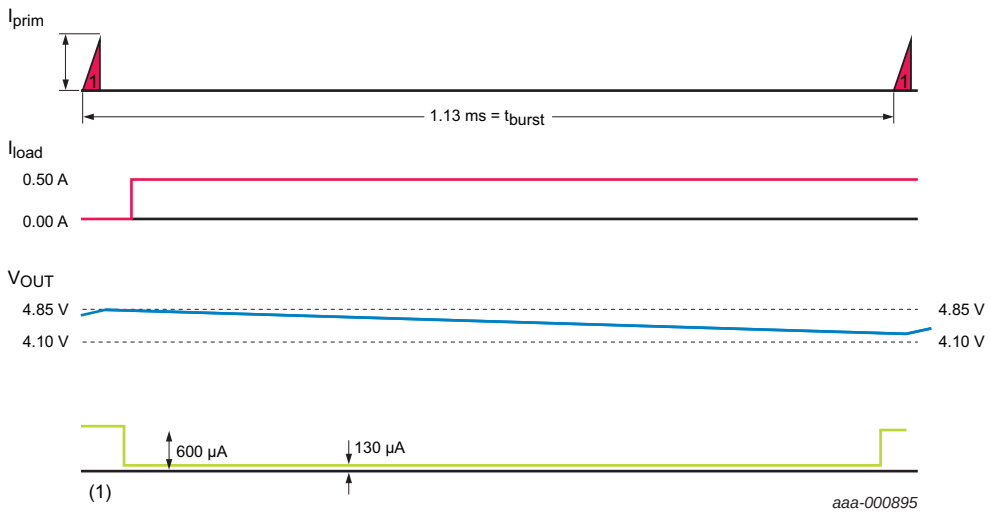
At fixed time intervals, the burst period is started. Each burst period starts with one stroke at a fixed I_{pk} level. After the stroke, the voltage is sensed at the FB pin near the end of the secondary stroke. If the sensed voltage is equal or above 2.5 V, no additional strokes are made. The IC now enters energy save mode until the next burst period. If the sensed voltage at the FB pin is below 2.5 V, additional strokes are made. This action continues until the sensed voltage level on the FB pin rises above 2.5 V. Thereafter, the IC goes into energy save mode until the next burst period.



(1) Start of burst
(2) End of burst
(3) Minimum supply current for energy save. Only the oscillator active
(4) $V_{OUT(pk)}$ reaches control value in 1 or 2 cycles
(5) IC switches to minimum supply current, energy save
(6) IC switches to nominal supply just before new burst start.
Timing and currents given are for TEA1721BT version with a f_{burst} = 885 Hz

Fig 7. Burst mode with energy saving

The fixed time interval between the start of the burst period enables the calculation of the required output capacitor to fulfill the load step of the USB 1.1 specification (V_{OUT} > 4.1 V for I_{OUT} load step from 0 => 0.5 A). The primary sensing concept cannot detect any changes on secondary side while the IC is not switching. During the time between burst periods, the output capacitor has to manage the load changes.



Timing and currents given are for TEA1721BT version with a f_{burst} = 885 Hz

Fig 8. V_{OUT} for load step occurring between burst periods

First when the next burst starts, the output voltage is monitored and the mode changes to provide for the increased load.

To speed up the change from burst mode to a higher power mode, the IC immediately switches from CVB mode to CVC mode once the release threshold voltage on the FB pin ($V_{th(rel)FB}$) is less than 2.4 V.

Low no-load power is achieved by:

- A low burst period repetition rate
- Switching the IC to energy saving mode between the burst periods. This action reduces current consumption by a factor of 5.

Reduced audible noise is achieved by:

- Selecting the minimum I_{pk} ($I_{pk(min)}$) for burst mode
- Using a 22.5 kHz repetition rate of the strokes within the burst period. This frequency is above the audible limit.

No-load power decreases as a longer time interval between burst periods is selected. However, using longer time intervals the output capacitor increases to compensate for the load steps that occur between burst periods.

An overview of available burst frequencies, no-load power and output capacitor value is given in Table 2 f_{burst} versus C_{out} and $P_{IN(no-load)}$.

When the output load increases, more strokes per burst period are added to transfer enough energy. Finally, the whole burst period is filled with strokes and the IC is switching continuously. When the load increases further, the IC goes into the next mode, CVC.

P_o in burst mode is calculated using Equation 2

$$P_o = 0.5 \times L_p \times I_{pk(min)}{}^2 \times f_{burst} \times average\ number\ of\ strokes \times \eta \quad (2)$$

Where:

- f_{burst} = the fixed burst frequency, determining the fixed time between bursts
- $I_{pk(min)}$ = the fixed minimum I_{pk} level in burst

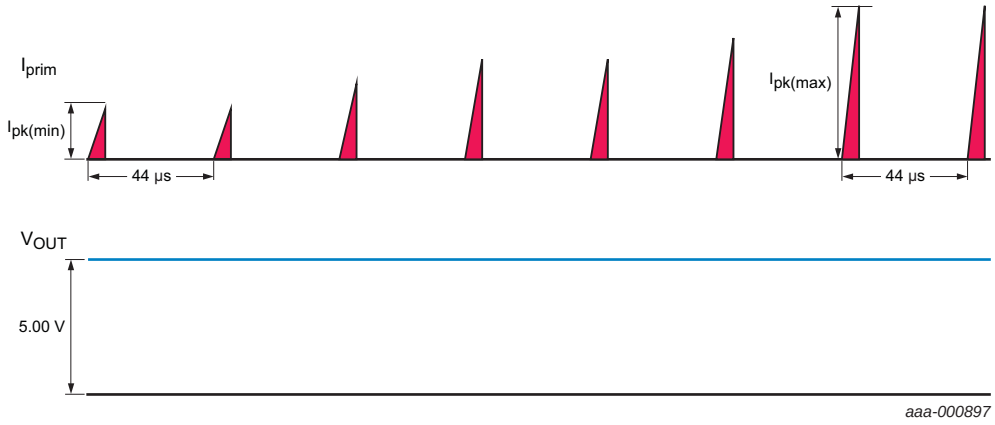
The level of I_{pk} is determined by measuring the voltage over the resistor from SOURCE pin to ground. The peak level, when measured in an application with an oscilloscope, is approximately 120 mV. This measured level includes internal propagation delay and differs from the value, given in the data sheet.

Remark: When the number of strokes in the burst period increases, the exact quantity of strokes can vary per burst period. This state is normal behavior in this mode. The average number of strokes over more burst periods is regulated to deliver the required output power.

5.3.2 CVC mode

CVC mode starts immediately after burst mode ends. The IC continuously switches at 22.5 kHz = f_{min} and peak current is equal to $I_{pk(min)}$. f_{min} is the minimum switching frequency in continuous mode.

When more output power is needed, switching frequency f_{min} (22.5 kHz) is maintained constant and the I_{pk} level is increased to deliver more power.



Remark: The on-time (t_{on}) increases with the amplitude of I_{pk}, which is not shown on these simplified graphs.

Fig 9. CVC mode with I_{pk} control

In this mode, the peak voltage level on the SOURCE pin increases from 120 mV to 565 mV. (Levels measured in an application with an oscilloscope, inclusive of propagation delay. Differs from the data sheet).

P_o in CVC mode is calculated using Equation 3.

$$P_o = 0.5 \times L_p \times I_{pk}^2 \times f_{min} \times \eta \quad (3)$$

Where:

- I_{pk} = Varying from $I_{pk(min)}$ to $I_{pk(max)}$, a result of $V_{SOURCE(pk)}$ changing from 120 mV to 565 mV on the SOURCE pin.
- f_{min} = Minimum switching frequency in continuous mode (22.5 kHz)

At $I_{pk(max)}$, the IC switches to CVF mode.

5.3.3 CVF mode

In CVF mode, I_{pk} is maintained constant on $I_{pk(max)}$ and the frequency is increased to deliver the additional required power.

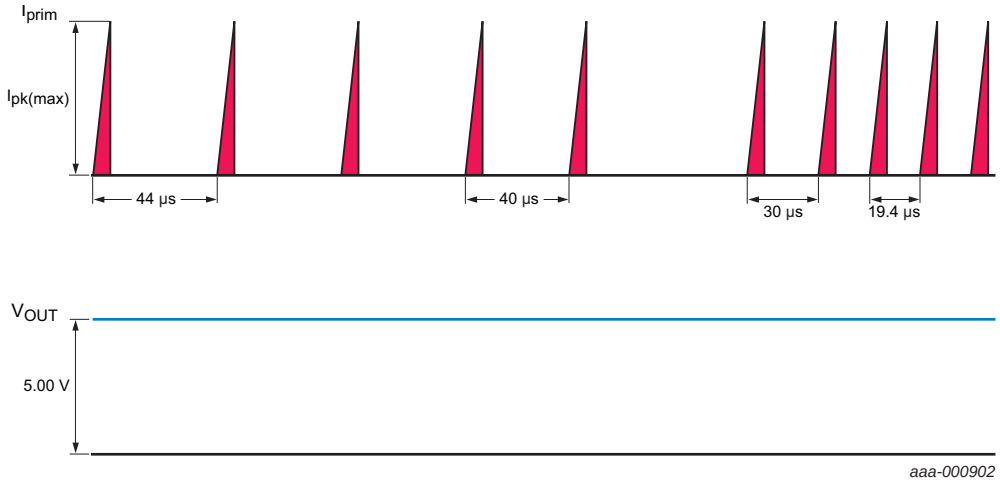


Fig 10. CVF mode with frequency regulation

The switching frequency increases in this mode from f_{min} (22.5 kHz) to f_{max} (51.5 kHz).

Output power is calculated using Equation 4

$$P_o = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{sw} \times \eta \quad (4)$$

Where:

- $I_{pk(max)}$ = Fixed maximum I_{pk} ($V_{SOURCE(pk)}$ on SOURCE pin 565 mV)
- f_{sw} = Switching frequency varies from f_{min} (22.5 kHz) to f_{max} (51.5 kHz)

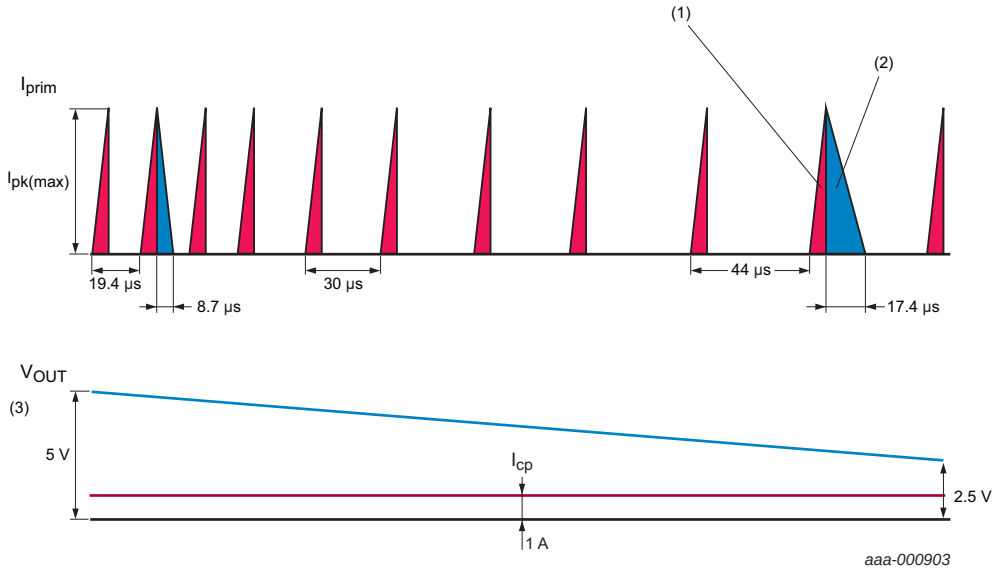
Maximum output power is calculated using Equation 5

$$P_{o(max)} = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{max} \times \eta \quad (5)$$

This formula is useful for dimensioning the circuit as used in Section 6.3. When the maximum power is exceeded, the IC switches to CCF mode.

5.3.4 CCF mode

CCF mode is the first Constant Current (CC) mode. In CC mode, the current is kept constant at $I_{OUT(max)}$. V_{OUT} varies with the equivalent resistive load value. For a linear decreasing resistive value of the load, V_{OUT} also decreases linearly. The CC mode is intended to charge batteries.



(1) Primary current, hot side

(2) Secondary current, cold side

(3) The converter operates in CCF for V_{OUT} from 5.3 V to 2.5 V and delivers 1 A to the charging port

Fig 11. CCF mode regulation by frequency

The output power formula is the same as for CVF mode, see Equation 6

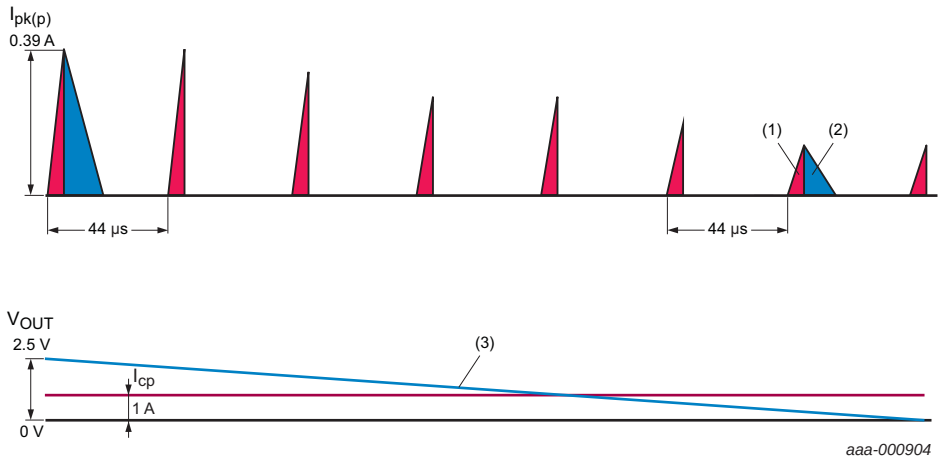
$$P_o = 0.5 \times L_p \times I_{pk(max)}^{2} \times f_{sw} \times \eta \quad (6)$$

Now f_{sw} is used to maintain I_{OUT} constant, while V_{OUT} becomes the voltage over the load at $I_{OUT(max)}$. f_{sw} drops from f_{max} (51.5 kHz) to f_{min} (22.5 kHz) while decreasing the resistive value of the load.

When f_{min} is reached, the IC switches to CCC mode.

5.3.5 CCC mode

In CCC mode, the switching frequency is maintained constant while the I_{pk} value is reduced. The I_{pk} value is regulated to maintain $I_{OUT(max)}$ constant.



(1) Primary current, hot side

(2) Secondary current, cold side

(3) In most applications, the converter operates in start-stop cycles for V_{OUT} < 1 V because the auxiliary winding VCC < $V_{CC(stop)}$.

Fig 12. CCC mode regulation by I_{pk}

Output power is calculated using Equation 7

$$P_o = 0.5 \times L_p \times I_{pk}^{2} \times f_{min} \times \eta \quad (7)$$

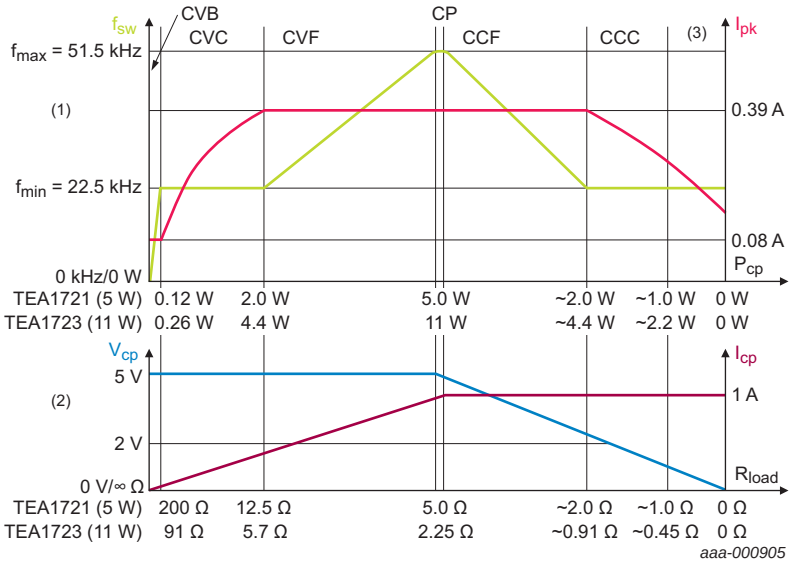
To keep $I_{OUT(max)}$ constant, I_{pk} is reduced from $I_{pk(max)}$ to $I_{pk(min)}$ while the resistive value of the load is further decreased.

Reducing the resistive value of the load reduces V_{OUT}. The auxiliary winding voltage, which is related to V_{OUT}, also drops. When the auxiliary winding voltage, supplying VCC, drops below $V_{CC(stop)}$, the IC stops and performs a restart. The IC remains in hiccup mode until the resistive value of the load is high enough to enable VCC supply above $V_{CC(stop)}$.

The moment $V_{CC(stop)}$ is reached, depends on the transformer construction and the supply circuit.

5.3.6 Overview control modes

Figure 13 summarizes the control modes.



(1) I_{pk} and f_{sw} as a function of P_{cp} (power to charging port)

(2) V_{cp} and I_{cp} as a function of R_{load} (load impedance to charging port)

(3) When V_{OUT} gets very low, VCC drops below $V_{CC(stop)}$ and IC enters hiccup mode

Fig 13. Overview control modes

The control graph is symmetrical, with both V_{OUT} on the left and I_{OUT} on the right constant.

5.4 Relationship between no-load and max load

As most of the parameters are fixed inside the IC, the different control modes and output power are all interdependent. The following summarizes the relevant formulas.

Burst mode:

$$P_o = 0.5 \times L_p \times I_{pk(min)}^2 \times f_{burst} \times average\ number\ of\ strokes\ per\ burst \times \eta \quad (8)$$

CVF mode ($P_{o(max)}$ is reached for f_{max})

$$P_o = 0.5 \times L_p \times I_{pk(min)}^2 \times f_{sw} \times \eta \quad (9)$$

For burst mode, $P_{IN(min)}$ is calculated using Equation 10. $P_{IN(min)}$ is reached at one stroke per burst period, excluding the efficiency:

$$P_{IN} = 0.5 \times L_p \times I_{pk(min)}^2 \times f_{burst} \quad (10)$$

For CVF $P_{o(max)}$ is defined as:

$$P_o = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{max} \times \eta \quad (11)$$

Except for L_p and the value for I_{pk}, all parameters (f_{burst}, f_{max}, ratio $I_{pk(min)}$, $I_{pk(max)}$) are fixed in the IC. Therefore, the ratio between $P_{o(max)}$ and $P_{IN(min)}$ is fixed. As $P_{o(max)}$ is a spec point, start with selecting L_p and $I_{pk(max)}$ so that $P_{o(max)}$ can be reached.

$P_{IN(min)}$ follows from the values chosen for $P_{o(max)} = \eta \times P_{IN(max)}$.

Using $P_{IN(max)} = \frac{P_{o(max)}}{\eta}$ Equation 12 can be written.

$$P_{IN(min)} = (P_{o(max)} \div \eta) \times (I_{pk(min)} \div I_{pk(max)})^2 \times (f_{burst} \div f_{max}) \quad (12)$$

Example:

In the following example, the results from a 5 W charger with an efficiency of 75 % are used.

Main parameter:

- L_p = 1.75 mH
- $I_{pk(max)}$ = 0.39 A => $I_{pk(min)}$ / 4.9 = 0.080 A
- f_{max} = 51.5 kHz
- f_{burst} = 885 Hz

$$P_{o(max)} = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{max} \times \eta = 0.5 \times 1.75 \times 10^{-3} \times 0.39^2 \times 51.5 \times 10^3 \times 0.75 = 5.14\ W \quad (13)$$

For a no-load condition, input power $P_{IN(min)}$ is of interest.

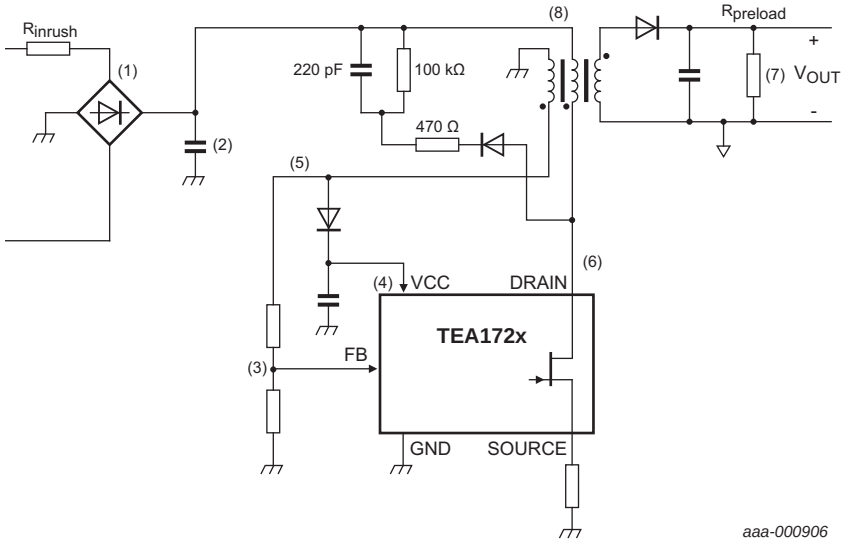
$$P_{IN(min)} = 0.5 \times L_p \times I_{pk(min)}^2 \times f_{burst} = 0.5 \times 1.75 \times 10^{-3} \times 0.080^2 \times 885 = 0.005\ W \quad (14)$$

To remain in regulation, occasional additional strokes are made in the burst period. In practice $P_{IN(min)}$ is about 40 % higher, at approximately 7 mW.

Remark: The total $P_{IN(min)}$ is higher due to additional losses in the circuit. These losses are described in Section 5.5.

5.5 Total input power at no-load

The calculated input power $P_{IN(min)}$ at no-load is only from the converter and at a minimum input voltage. In an actual application, there are additional losses present. All no-load losses are shown in Figure 14.



(1) Rectifier 0.1 µA (40 °C), 325 V, 2 × 0.1 mW

(2) Electrolytic capacitor 10u 400 V 10 µA, 375 V (estimation) 3.5 mW

(3) FB sensing, only dissipating during pri + sec stroke, 0.1 mW

(4) VCC = 12 V, I = 0.1 mA, 3 mW

(5) Snubber 2 mW

(6) Leakage HV current source, 1 µA, 375 V, 0.4 mW

(7) V_{sec} = 5 V, I = 0.8 mA, 4 mW

(8) The minimum transferred energy ($f_{burst} \times 0.5 \times L_p \times I_{pk(min)}^2$, only one cycle per burst) is divided between the VCC supply and the preload.

Fig 14. No-load losses

The input power is higher in practice due to the additional losses:

- Increase of I_{pk} at higher input voltage (IC has no V_{IN} compensation). The difference between 85 V (AC) and 264 V (AC) is about an additional 2 mW
- Leakage main electrolytic capacitor (3.5 mW)
- Leakage bridge diodes, leakage high-voltage start-up current source (0.5 mW)
- Snubber losses (2 mW)

Combining the additional losses, $P_{IN(min)tot}$ at no-load for f_{burst} = 885 Hz equals:

$P_{IN(min)tot} = 7 + 2 + 3.5 + 0.5 + 2 = 15$ mW

f_{burst} determines the value of $P_{IN(min)}$, a lower f_{burst} leads to a lower $P_{IN(min)}$. However, other losses including, electrolytic capacitor leakage, diode bridge leakage must be minimized to achieve low no-load power.

For the lowest burst frequency of 420 Hz, the calculation is as Equation 15:

$$P_{IN(min)} = 0.5 \times L_p \times I_{pk(min)}^{2} \times f_{burst} = 0.5 \times 1.75 \times 10^{-3} \times 0.080^{2} \times 420 = 0.0024\ W \quad (15)$$

Practical value (in regulation) $P_{IN(min)}$ is 40 % higher at 3.4 mW.

The additional losses are lower when they are related to f_{burst}:

- Increase of I_{pk} at higher input voltage (IC has no V_{IN} compensation). The difference between 85 V (AC) and 264 V (AC) is about an additional 1 mW
- Leakage main electrolytic capacitor (3.5 mW)
- Leakage bridge diodes, high-voltage start-up current source (0.5 mW)
- Snubber losses (1 mW)

$P_{IN(min)tot}$ = 3.4 + 1 + 3.5 + 0.5 + 1 = 9.4 mW

For an overview of burst frequencies, see Table 2

5.6 Relationship between f_{burst} and output capacitor

The USB 1.1 specification (see Section 7.1.1) requires that V_{OUT} remains above 4.1 V for a load step of 0 A => 0.5 A. This condition is critical in burst mode as the primary sensing concept is "blind" of conditions on the secondary side while the IC is in energy save mode.

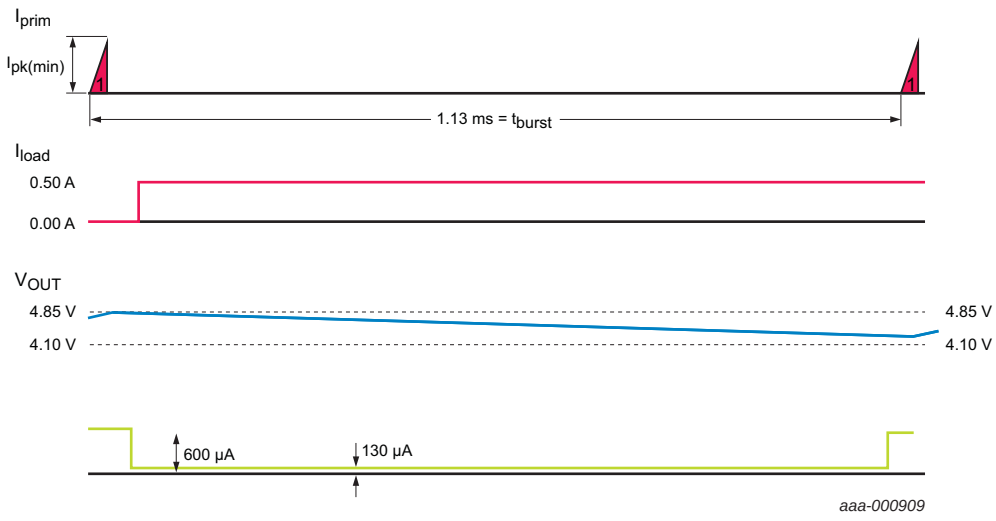


Fig 15. f_{burst} and output capacitor

The worst case is when the load step occurs as the IC enters energy save mode. The maximum time the capacitor has to maintain the output voltage is $1/f_{burst}$.

The capacitor value can be calculated using Equation 16:

$$C = I_{load} \div (f_{burst} \times V_{drop}) \quad (16)$$

Where:

- I_{load} = current after load step
- V_{drop} = V_{OUT} at the beginning of load step −4.1 V

The formula indicates the relationship between burst frequency f_{burst}. and the output capacitor. A lower f_{burst} leads to a lower $P_{IN(min)tot}$ at no-load, but needs a larger output capacitor to fulfill the load step requirement.

Example:

Due to the internal load line, V_{OUT} drops when the load increases. V_{OUT} must remain higher than 4.75 V. Therefore, V_{OUT} at no or low load during burst is always higher than the specified minimum V_{OUT} voltage of 4.75 V. In practice, the lowest V_{OUT} in burst where no-load step is detected, is 4.85 V.

As a result, the voltage on the output capacitor can drop from 4.85 V to 4.1 V.

- V_{drop} = 0.75 V
- I_{load} = 0.5 A

Equation 17 show the calculated value of C_{out} for an f_{burst} of 885 Hz:

$$C_{out(min)} = 0.5 \div (885 \times 0.75) = 753 \times 10^{-6} \quad (17)$$

The results in Equation 17 represents the minimal required value for the capacitor (C). As most electrolytic capacitors have a tolerance of −20 % on the low-side, divide the calculated value by 0.8 to obtain the nominal value. See Equation 18

$$C_{out(nom)} = 753 \times 10^{-6} \div 0.8 = 941 \times 10^{-6} \quad (18)$$

Table 2 provides an overview of the (nominal) output capacitor value related to the burst frequency and no-load P_{IN}.

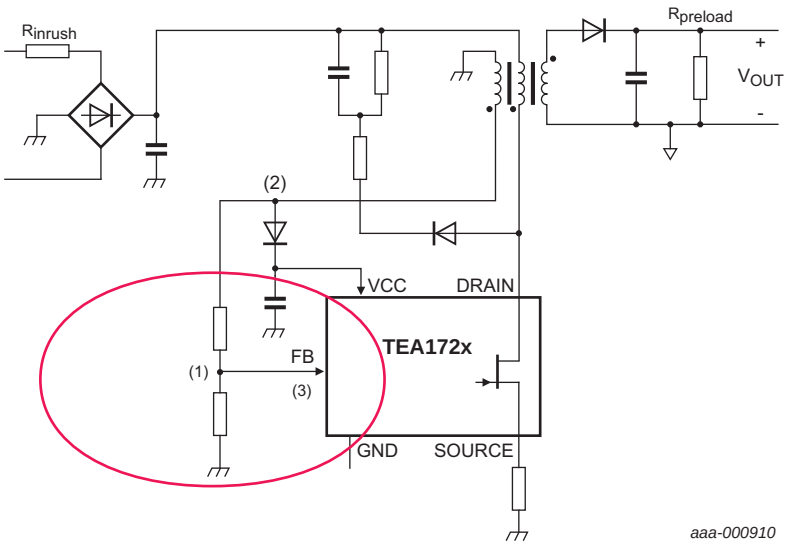
Table 2. f_{burst} as a function of C_{out} and $P_{IN(no-load)}$

f_{burst}	$C_{out(nom)}$	$P_{IN(no-load)}$	
		TEA1721	**TEA1723**
420 Hz	2 × 1000 µF	< 10 mW	< 17 mW
885 Hz	2 × 470 µF	< 16 mW	< 26 mW
1260 Hz	680 µF	< 22 mW	< 35 mW
1750 Hz	2 × 820 µF	< 33 mW	< 50 mW

The version with f_{burst} = 1750 Hz with large output capacitance is intended for applications with high requirements for the load step behavior.

5.7 Feedback

In a primary sensed system, the output voltage is regulated by measuring the voltage of an auxiliary winding on primary side.



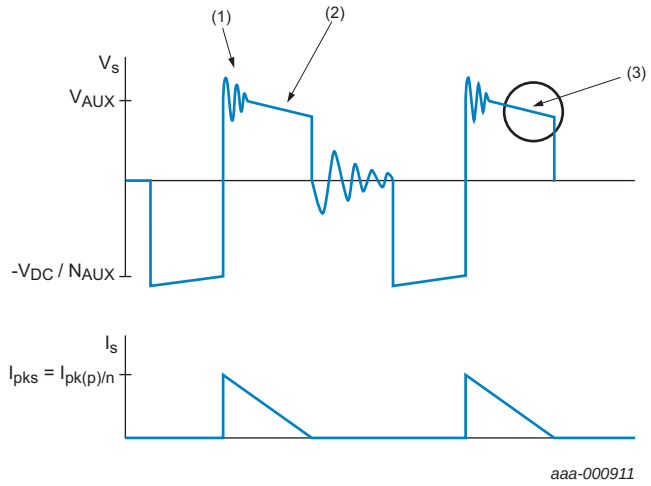
(1) Primary sensing via auxiliary winding
(2) Auxiliary winding also provides VCC
(3) Regulation level on FB pin is 2.5 V

Fig 16. Feedback from auxiliary winding

For optimal matching of the auxiliary winding voltage and the output voltage, tightly couple the transformer auxiliary winding to the secondary winding.

Due to the primary sensing concept, the secondary voltage is regulated before the secondary diode. Changes in voltage drop over the diode are not corrected and are reflected in the V_{OUT} level.

Figure 17 shows the waveform on the auxiliary winding.



(1) No accurate measurement possible during ringing

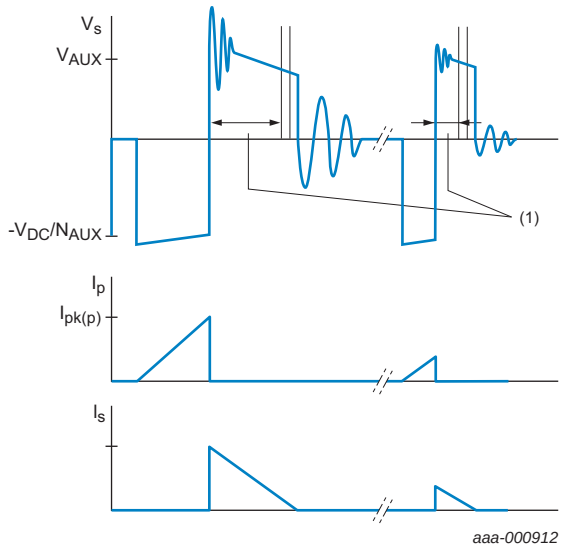
(2) Voltage drops due to decreasing voltage over the secondary diode with decreasing current

(3) Measurements done towards the end of the secondary stroke at minimal secondary current to increase accuracy and avoid ringing.

Fig 17. Auxiliary winding waveform

V_{OUT} is measured during the secondary stroke. To increase the accuracy, V_{OUT} is sampled near the end of the secondary stroke. This timing minimizes the influence of the voltage drop over the secondary diode because the diode current is close to zero. It also minimizes the error, due to ringing.

As the secondary stroke time varies with the value of I_{pk} (the higher I_{pk}, the longer the secondary stroke time), the sample time is adapted accordingly.



(1) To increase measurement accuracy, the position of the measurement pulse is adapted to the duration of the secondary stoke. A measurement is taken near the end of the stroke where the secondary stroke is close to zero and ringing is minimal

Fig 18. Adaptive sample time

Configure the resistive divider on the FB pin to deliver 2.5 V at the FB pin near the end of the secondary stroke in burst mode. Take into account that the voltage near the end of the secondary stroke is $V_{OUT} + V_{diode}$.

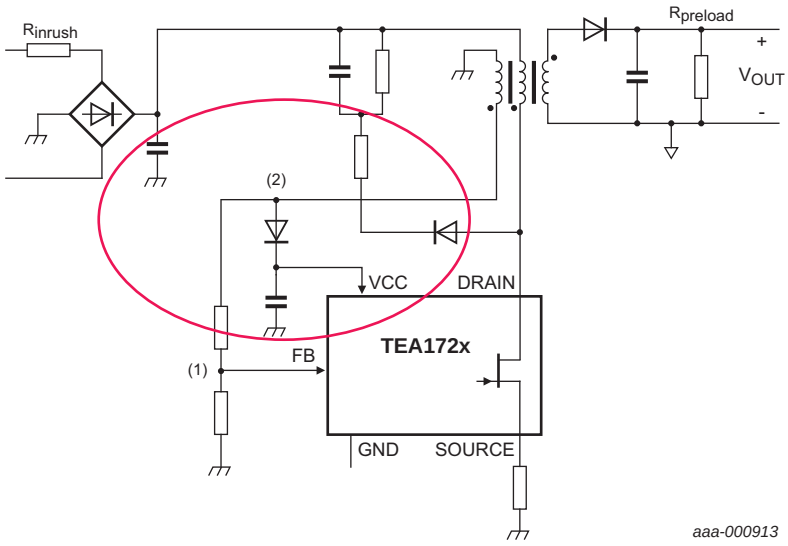
5.8 Demagnetization protection

The signal of the auxiliary winding on the FB pin is also used for demagnetization protection. That is, to determine if the secondary stroke has ended and all stored energy in the transformer is transferred to secondary winding.

To release the demagnetization protection, the voltage on the FB pin must drop below 50 mV after the secondary stroke has started. When no demagnetization is detected, the next primary stroke is prohibited until demagnetization is true. This condition guarantees discontinuous operation.

5.9 Supply from the auxiliary winding

The supply of the IC is supplied from an auxiliary winding. It is possible to use the feedback auxiliary winding or a separate winding.

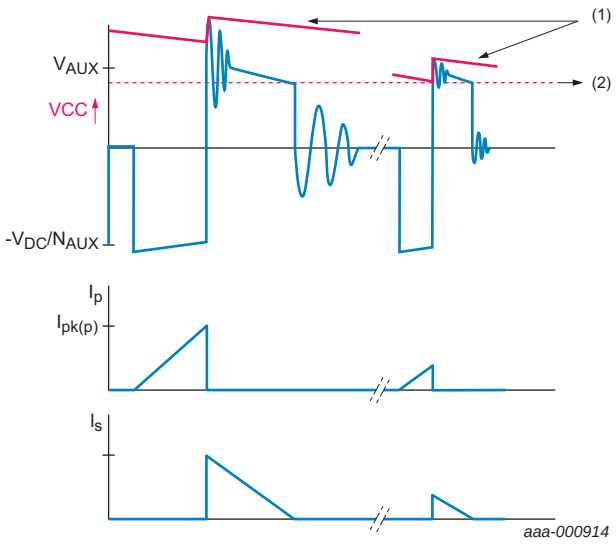


(1) Primary sensing via auxiliary winding

(2) Auxiliary winding also provides VCC

Fig 19. Supply from the auxiliary winding

When designing the auxiliary winding, consider the waveforms on the winding as shown in Figure 20:



(1) Actual VCC, resulting from peak rectification of the ringing

(2) VCC, expected from the transformer calculations using winding ratio's

Fig 20. VCC higher than anticipated due to ringing

As the power consumption of the IC is low, the rectified voltage of the auxiliary winding follows the peak of the ringing (peak rectification). Therefore, the supply voltage is much higher than anticipated.

The amount of ringing depends on the coupling of the auxiliary winding with the primary and secondary winding. As necessary, adapt the number of auxiliary windings to obtain the correct supply voltage.

The supply voltage range is large, approximately 8.5 V to 35 V. For optimum efficiency and no-load input power, design VCC for 10 V to 12 V at no-load.

As the ringing increases for higher loads, demo board VCC rises from 12 V at no-load to 22 V at maximum load.

5.10 Soft start

To reduce stress at start-up, the IC starts in CC mode with reduced I_{pk}. The output current is limited to 1 A during start-up. Charging of the output capacitor of 2 × 470 μF takes less than 5 ms.

5.11 Load line compensation

For stable regulation, it is necessary that the voltage on the FB pin drops for higher loads. This leads to a load line from zero load to full load of 450 mV. The IC has a built-in load line compensation that limits the load line from zero to full load below 200 mV.

5.12 Jitter

To improve ElectroMagnetic Interference (EMI), the switching frequency varies around the center value. This results in reduced peak levels around the switching frequency. Jitter is present in all modes and amounts approximately ±8 %. The jitter frequency is between 100 Hz to 400 Hz. To keep P_o constant while varying f_{sw}, I_{pk} is adapted accordingly as can be derived using Equation 19.

$$P_o = 0.5 \times L_p \times I_{pk}^{2} \times f_{sw} \times \eta \quad (19)$$

5.13 Protective features

The following protective features are implemented:

- UnderVoltage Protection (UVP) on the VCC pin
- OverVoltage Protection (OVP) V_{OUT} (via FB pin)
- OverTemperature Protection (OTP)
- Demagnetization protection
- Open/short circuit protection on the FB pin

The IC can also handle a short-circuit on the secondary side in a safe way. The behavior is described in Section 6.5.

5.13.1 UnderVoltage Protection (UVP) on the VCC pin

The UVP on the VCC pin prevents unpredictable behavior when the supply voltage drops below the minimum level needed for operation. The UVP level and action taken are as follows:

- UVP: VCC < 8.5 V restarts the IC

Restart causes switching to stop and the high-voltage current source is enabled to charge the VCC capacitor. When VCC rises above 17 V ($V_{CC(startup)}$), the high-voltage current source is disabled and switching restarts.

If an error persists, the sequence repeats itself. This condition is known as “hiccup mode”.

5.13.2 OverVoltage Protection (OVP) on V_{OUT}

The voltage on secondary side is monitored using V_{FB} (measured on the FB pin). Under normal operation, the V_{FB} is approximately 2.5 V when sampled during the secondary stroke. If V_{FB} > 3.2 V, a forced restart is performed.

- OVP secondary side: Sampled voltage on pin FB > 3.2 V causes the IC to restart

When the sampled voltage on pin FB > 3.2 V, switching stops. The auxiliary winding no longer provided the VCC supply and VCC drops. When required, the IC waits until the VCC supply < 8.5 V before enabling the high-voltage current source to charge the VCC capacitor.

When $V_{CC(startup)}$ > 17 V, the high-voltage current source is switched off and the switching is re-enabled. If the error persists and the sampled voltage on pin FB > 3.2 V, switching stops, the sequence repeats itself. This condition is known as “Hiccup mode”.

The level of overvoltage is calculated as follows:

- Sampled voltage FB pin for V_{OUT} = 5 V: 2.5 V
- Voltage on secondary winding before the diode: 5.3 V
- Ratio voltage secondary winding divided by the sampled voltage the FB pin = 5.3 V / 2.5 V = 2.12
- Voltage (secondary winding) for the sampled voltage FB = 3.2 V: 3.2 V × 2.12 = 6.8 V

The output voltage must rise above 6.8 V before OVP is triggered. In practice, OVP triggers at an output voltage between 6.5 V and 6.8 V. However, it depends on the steepness of the V_{OUT} increase.

5.13.3 OverTemperature Protection (OTP)

When the temperature of the IC increases above 150 °C, OTP is activated. The IC stops switching and VCC drops. When VCC falls below the $V_{CC(stop)}$ of 8.5 V, the high-voltage current source charges the VCC capacitor until 17 V ($V_{CC(startup)}$). The IC does not start switching until the die temperature drops < 100 °C. During the waiting time, VCC cycles between charging to $V_{CC(startup)}$ then discharges to $V_{CC(stop)}$.

The hysteresis from 150 °C to 100 °C ensures that no dangerous situations occur.

5.13.4 Demagnetization protection

Demagnetization protection is implemented to check that the secondary stroke has ended before enabling the next primary stroke. This condition ensures discontinuous operation and prevents stress in overload conditions.

5.13.5 FB pin open and short-circuit protection

The FB pin detects if there is an AC voltage present on the pin. When the voltage on the pin does not alternate below and above 50 mV, switching is stopped. This action prevents the presence of an uncontrolled output voltage when the FB pin is open or shorted to ground.

5.13.6 Protection features overview table

Table 3. Protection feature overview

Protection feature	Level	Action
VCC UVP	8.5 V	restart
V_{OUT} OVP	V_{FB} pin > 3.2 V	restart
OTP	150°	stop switching until T < 100 °C
Demagnetization	V_{FB} < 50 mV	hold next primary stroke until demagnetization has occurred
FB pin open and short-circuit	AC detection FB pin	stop switching

6. Application

6.1 Application diagram

Figure 21 shows the demo board schematic configured as a 5 W charger application. Following the schematic each component from the AC input to the output stage is explained. At the end of this section the schematic of an 11 W charger is given. Also the main differences with the 5 W application are described.

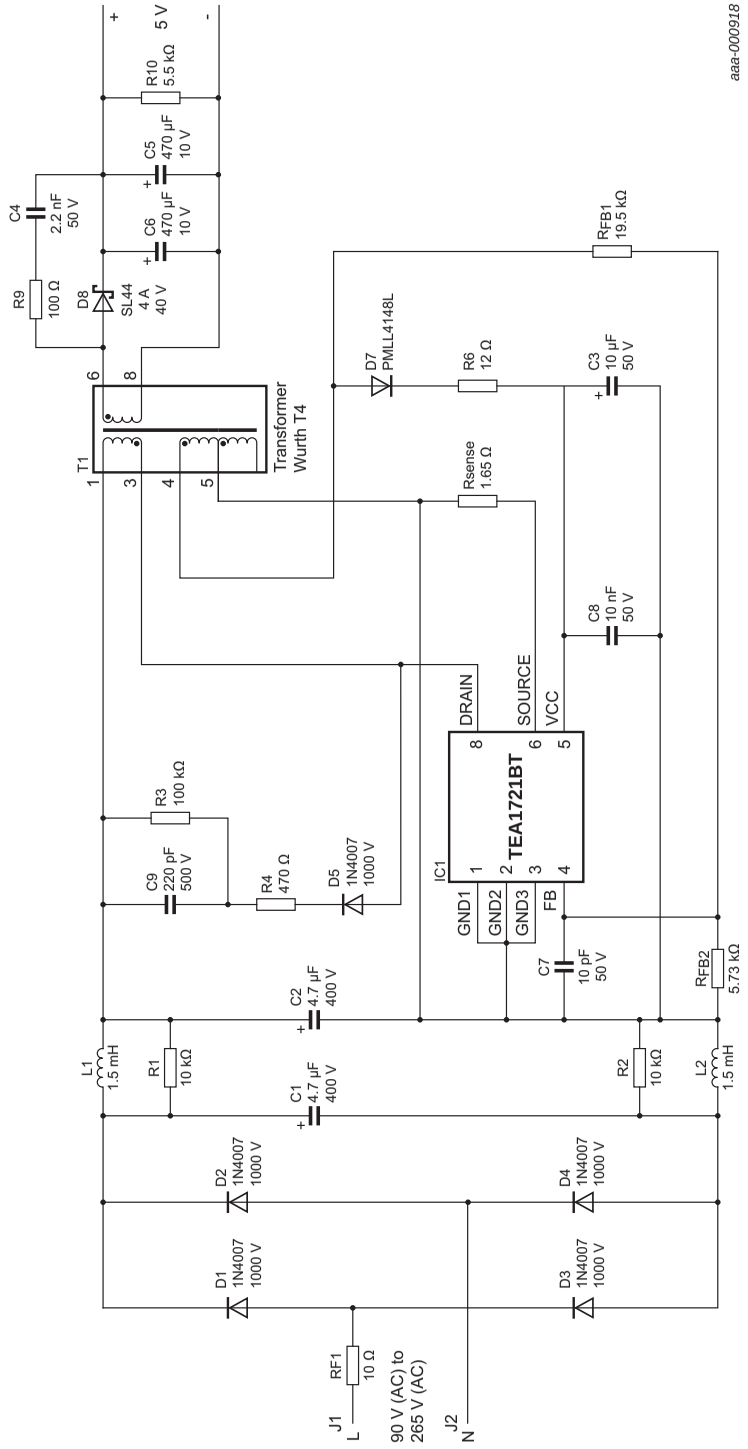


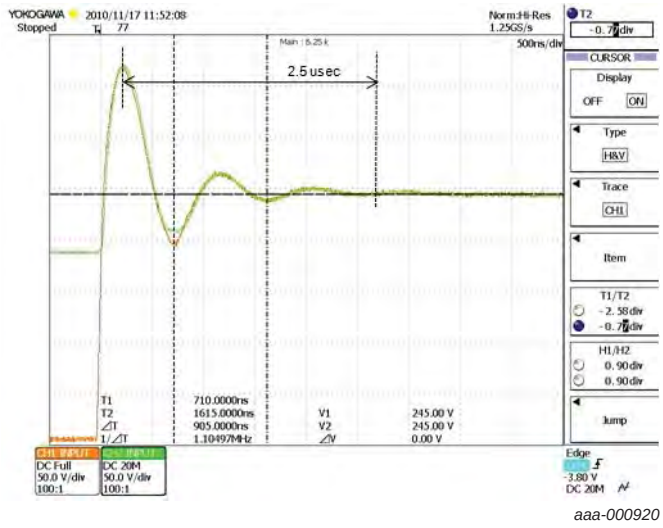
Fig 21. Demo board schematic (5 W)

6.1.1 Input and EMI filter

Figure 21 shows fuse resistor RF1 that is part of the input circuit. RF1 is a 2 W fusible resistor designed to limit the inrush current and provides primary side short-circuit protection. For mains rectification, standard diodes are used, however the use of a diode bridge is also possible. Capacitors C1 and C2 form the main electrolytic capacitor, C1, C2, L1, L2, R1, and R2 form the damping filter for conducted EMI.

6.1.2 Clamp

Diode D5, R4, R3 and C9 are designed to dampen the ringing after switch-off of the integrated MOSFET switch. D5 must be a slow diode for ringing damping. Figure 22 and Figure 23 show damping using fast and a slow diode.

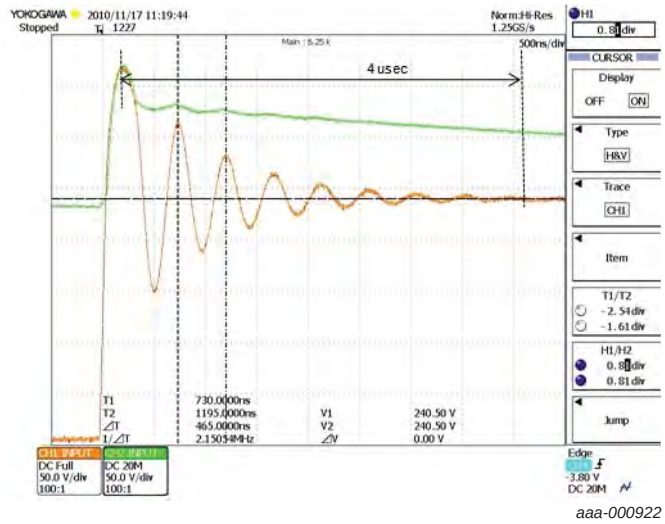


CH1 (Orange): Drain primary switch

CH2 (Green): Cathode clamp diode

Fig 22. Damping using a slow diode (1N4007)

Using a slow diode, the diode conducts after the drain signal reaches its peak and the clamping circuit remains parallel to the primary. This action leads to the fast damping of the ringing. The ringing frequency is 1.1 MHz, damping time is 2 µs.



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CH1 (Orange): Drain primary switch

CH2 (Green): Cathode clamp diode

Fig 23. Damping using a fast diode (BYW26CV)

Using a fast diode, the clamping capacitor remains charged after reaching a peak, the clamping circuit is not active and does not provide further damping. The oscillation frequency is 2.2 MHz and the damping time increases to 4 µs. Quick damping of the oscillation is important to ensure proper measurement of the voltage on the FB pin at the end of the secondary stroke.

The value of R4 controls the damping and is a compromise of the damping speed and the additional dissipation of the clamp. The values shown are a good starting point for a 5 W application.

6.1.3 Source resistor

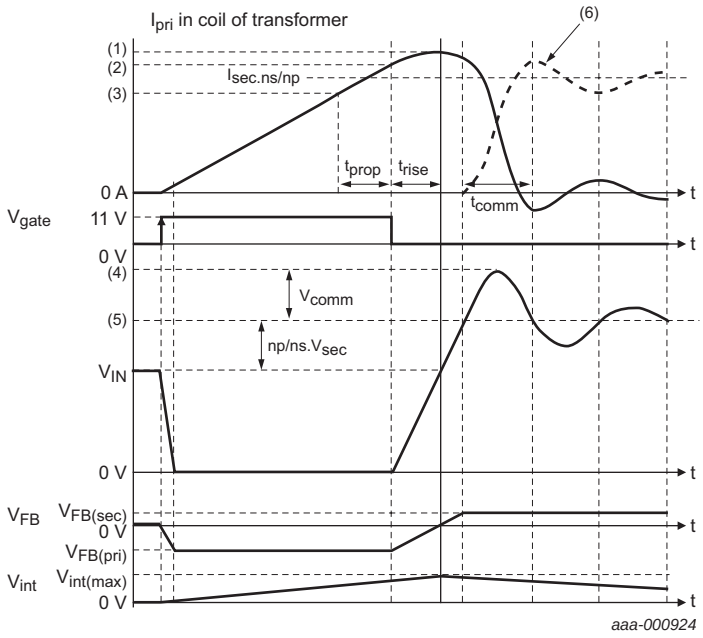
The source resistor between SOURCE pin and ground comprise three SMD resistors in parallel. Parallel configuration allows the use of standard SMD resistors for accurate tuning. The value of the source resistor is calculated as follows:

$$R_{SOURCE} = V_{SOURCE(pk)max} / I_{pk(p)max}$$

$V_{SOURCE(pk)max}$ = 0.565 V and $I_{pk(p)max}$ is the peak current required to deliver full power as in the following calculation:

$$P_{IN(max)} = 0.5 \times L_p \times I_{pk(max)}^2 \times f_{max}$$

In practice, R_{SOURCE} can be about 5 % larger as the real I_{pk} continues to increase after switch-off from the MOSFET.



(1) I_{pk} (V_{DRAIN} = V_{IN})

(2) I_p (V_{GATE} = 0 V

(3) I_p (V_{SOURCE} = V_{pk})

(4) V_{IN} + nV_{sec} + V_{comm}

(5) V_{IN} + nV_{sec}

(6) I_{sec} ns/np in secondary coil of transformer

Fig 24. Detail rise of the primary circuit

After reaching the internal V_{pk} level of the control loop, there is an internal delay (t_{PD} = propagation delay) before the gate is turned off. The value shown for $V_{SOURCE(pk)max}$ is taking this propagation delay into account, as it is measured in a practical application.

After the gate is turned off, I_p increases until the voltage over the primary coil is zero. Under theses conditions, the voltage on the drain equals V_{IN}.

The exact amount of overshoot of I_{pk} depends on the steepness of the primary current rise. Some tuning of R_{sense} could be necessary.

6.1.4 Auxiliary winding supply

The auxiliary winding of the transformer supplies the IC VCC voltage via D7, R6 and C3. The peak of the ringing (peak rectification) determines the VCC level and not the average level of the secondary stroke. Resistor R6 is used to prevent a too heavy short load of the auxiliary winding under no-load conditions. A short load can disturb the sampling of the voltage at the FB pin. If the output voltage drops below 1 V, resistor R6 can be trimmed to ensure the IC switches off when in current mode. As VCC runs on peak rectification, it is possible the IC continues operating up to an output voltage of 0 V.

Remark: Install capacitor C10 as close to the IC as possible to suppress disturbances.

6.1.5 Auxiliary winding: Feedback

The auxiliary winding is fed to the FB pin. The resistive divider consists of R7, R8, R13 and R14. To set an accurate division factor, use two resistors in parallel. Capacitor C7 is added for spike suppression. Select a low value for C7 (around 10 pF) to avoid a disruption of the waveform at the FB pin. A low value for C7 provides accurate sampling of the voltage.

6.1.6 Secondary side

On the secondary side, Schottky diode D8 is used for rectification. Despite a 1 A rated output current, the peak current can be higher than 4.5 A. Therefore, for efficiency select a diode able to manage a current higher than 4.5 A. Capacitor C4 and R9 suppress the switching spikes of the diode.

The output capacitors C5 and C6 manage the load step in burst mode. For output ripple and load step behavior, use capacitors with low Equivalent Series Resistance (ESR).

Table 4 summarizes the relationship between the value of the output capacitor, burst frequency and no-load power for a 5 W and 11 W application:

Table 4. f_{burst} versus C_{out} and $P_{IN(no-load)}$

f_{burst}	$C_{out(nom)}$	$P_{IN(no-load)}$	
		TEA1721	TEA1723
420 Hz	2 × 1000 μF	< 10 mW	< 17 mW
885 Hz	2 × 470 μF	< 16 mW	< 26 mW
1260 Hz	680 μF	< 22 mW	< 35 mW
1750 Hz	2 × 820 μF	< 33 mW	< 50 mW

Resistor R10 is the preload resistor. The preload resistor serves two purposes:

- A small load on secondary side ensures proper regulation of the output voltage at no-load condition.
- The preload resistor dissipates any excess of energy above the IC supply and the auxiliary divider generated in no-load conditions by the fixed burst frequency. If excess energy is not dissipated, the output voltage rises up to the OVP level.

6.2 Layout considerations

Layout is not critical, however for the best result the following items are taken into account:

- Separation of large signal and small signal path
- Copper area at ground pins for cooling
- Routing input filter
- Short connection secondary diode to transformer and output capacitor

Figure 25 show the layout of the demo board:

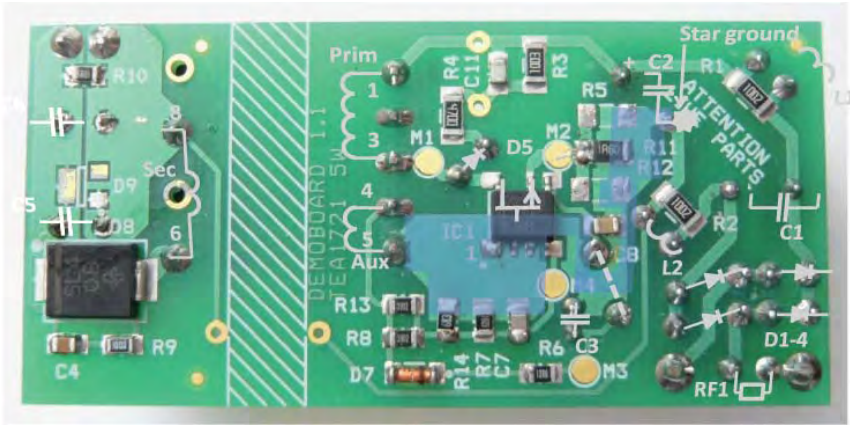


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Fig 25. Demo board layout (5 W)

Both components on top side and bottom side are shown for reference. The ground plane is emphasized with a transparent light blue color. For recognition, the internal switch of the IC between pin 7 and 6 is drawn. Figure 21 shows the circuit diagram.

6.2.1 Separation large and small signal path

The area above the IC carries the large currents and high voltages and the area below the IC is the small signal area. The negative pole of C2 acts as star ground where all grounds (large signal, small signal, AC input) merge.

The loop of the large signal current is kept small. When the internal switch is closed, the current flows from the plus terminal of C2 to the primary winding. Thereafter, the current flows via the internal switch between pins 7, 6 and the source resistor R5, 11,12 back to the minus terminal of C2, star ground. When the internal switch is off, the current of the primary winding flows into the clamp via diode D5, R4, R3 and C11 back to the positive terminal of C2 and (during rise of the drain voltage) via the parasitic capacitance of the internal switch and the source resistor to ground.

The small signal ground is positioned below the IC. Here the auxiliary winding is grounded. Via D7, R6, C3, a bridge wire and C8 the auxiliary winding supplies the VCC on pin 5. Via the resistive divider R8, R13 and R7, R14, C7 the signal of the auxiliary winding is fed to FB pin 4.

6.2.2 Cooling the IC

IC pins 1 to 3 are connected to a copper plane, and used for cooling the IC. The heat of the internal switch is conducted from the IC via pin 1 and 3. The heat transfer from the IC pins is optimized by using a contiguous copper plane underneath the pins. The holes in the silk screen create the solder islands for the IC pins. The size of the copper plane is 10 mm × 8 mm. This plane provides sufficient cooling of an enclosed 5 W application up to 45 °C.

6.2.3 Input filter

The input part is routed such that interference from switching cannot reach the mains connection without passing through the filter L1, L2 and C1. Crosstalk directly to the mains connections is avoided by creating sufficient spacing.

6.2.4 Secondary side

On the secondary side, a rectifier diode is placed as close as possible to the winding to improve EMI. In addition, the connection from cathode to output capacitor is as short as possible. R9 and C4 are added to suppress switching spikes. The position of preload resistor R10 is not critical.

6.3 Transformer

For proper functioning of the primary sensing concept, attention is needed for the correct transformer construction.

The considerations are as follows:

- L_p and I_{pk} in relation to input voltage and power
- Secondary stroke must be long enough for proper sampling of V_{OUT}
- Transformer construction of windings
- Safety

The following outlines the basics of transformer selection:

6.3.1 Calculation of L_p and I_{pk}

Figure 26 shows a calculation example for a 5 W application. Only the main items, which determine the transformer are calculated, the primary inductance L_p and the peak current I_{pk} at maximum output power.

At the right-hand side, the explanation of parameters and used formulas are given. Below some additional details of Figure 26 are described.

f_{mains}

f_{mains} the lowest mains frequency selected for this application is 60 Hz and not 50 Hz. The reason is 50 Hz mains have nominal voltages of 220 V or higher. A drop to 85 V is not realistic at these voltage levels.

Selection nV_{OUT}

The value of nV_{OUT} (the output voltage multiplied by the ratio of the number of primary windings and number of secondary windings) influences two design parameters:

- The peak voltage on the primary switch
- The secondary stroke time

The formula for the peak voltage on the primary switch when turned off is:

$$V_{pk(p)} = V_{elcap(max)} + nV_{OUT} + V_{pk(ringing)}$$

Where:

$V_{pk(p)}$ has to remain below the maximum breakdown voltage of the switch.

$V_{elcap(max)}$ is reached for maximum AC input voltage 264 V (AC) and is about 375 V (DC).

$V_{pk(ringing)}$ can run up to about 100 V.

By selecting nV_{OUT} not too high, $V_{pk(p)}$ can be maintained at a safe level.

	Input value			
	Calculated			
Fill in the required	**Values, pending on design**			
parameters in the	Vout	5.00	Vdc	Output voltage converter @ max load
green fields	Iout	1.00	A	Maximum output current converter
	Vf	0.60	V	Forward voltage secondary diode
	Cmains	9.40E-06	F	Value total elcap behind rectifier
	Vmains_min	85.00	Vac	Lowest specified mains input voltage for full performance
	Fmains	60.00	Hz	Frequency mains voltage @ minimal input voltage
	nVout	72.00	V	Practical value between 60 and 80 Volt, select highest value for which Tsec_min = 1.9 us
The other values are	**Values, fixed by IC design**			
fixed for this design	eff	0.75		Converter efficiency
	Fsw_max	5.20E+04	Hz	Switch frequency at max power
	Tdead_min_perc	0.05		1/Fsw = Tprim + Tsec + Tdead_min, Tdead_min to guarantee discontinuous operation
	Tdead_min	9.62E-07		Tdead_min = 1/Fsw * Tdead_min_perc
	Calculation minimal DC voltage at converter input			
	Pin	6.67	W	Pin = Vout * Iout_max / eff
	Vpeak_elcap	118.81	V	Vpeak_elcap = Vmains_min * SQRT(2) - 2 * drop over bridge diodes (0.7V / diode)
	Vmin_elcap	74.71	V	Vmin_elcap is where the dropping voltage of the elcap meets the rising mains voltage
				For the elcap voltage we can write for Tm, where Tm is the time after reching the Vpeak_elcap:
				0.5 * Cmains * (Vpeak^2 - Velcap^2) = Pin * Tm =>
				Velcap = SQRT((Vpeak^2) - ((Pin * Tm)/(0.5 * Cmains)))
				For the rising voltage of the mains the formula is:
				Vmains = Vpeak * sin (2*pi*Fmains*(Tm - 1/(4*Fmains)))
	Calculation Ipk, Lp			
				Derivation:
			1	Pin = Fsw_max * 0.5 * Lp * Ipk^2
			2	Pin = Pout/eff.
			3	Ipk = Vmin_elcap * Tprim / Lp
			4	Ipk = nVout * Tsec / Lp
			5	Tprim + Tsec + Tdead_min = 1/Fsw_max
				Substitute 3 and 4 in 5
				(Lp*Ipk)/Vmin_elcap + (Lp*Ipk)/nVout + Tdead_min = 1/Fsw_max
				Lp*Ipk = (1/Fsw_max - Tdead_min)(1/(1/Vmin_elcap + 1/nVout) = (1/Fsw_max)(1-Tdead_min_perc)(1/(1/Vmin_elcap + 1/nVout)
				Substitute Lp*Ip in 1
	Ipk	3.83E-01	A	Ipk = (2 * Pin * (Vmin_elcap + nVout)) / ((Vmin_elcap * nVout) * (1-Tdead_min_perc))
	Lp	1.75E-03	H	Lp = (1/Fsw_max - Tdead_min) * 1 / (1/Vmin_elcap + 1/nVout) * 1/Ipk
	Tsec_max	9.30E-06		Tsec = Lp * Ipk / (nVout)
	Tsec_min	1.90E-06		Tsec_min = Tsec_max * (Ipk_min/Ipk_max) = Tsec_max / 4.9

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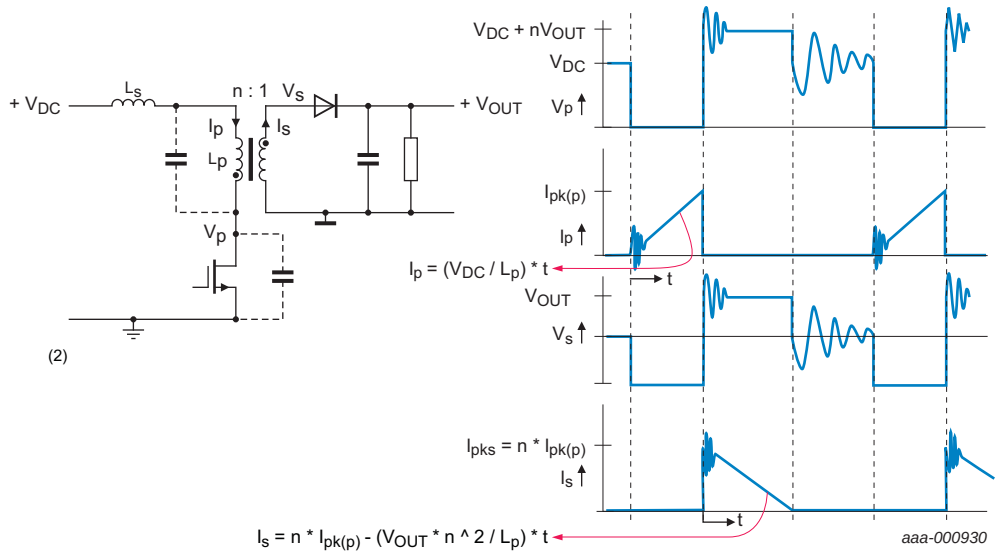
Fig 26. L_p and I_{pk} calculations (5 W)

6.3.2 Secondary stroke time

The sampling timing during the secondary stroke time is related to the output power. The secondary stroke time is also related to the output power, it is important that the sampling timing fits within the secondary stroke time. Figure 27 shows some basic signals and the relationship between secondary stroke time and the transformer.



(1) $I_{pk(p)}$ = primary peak current.

(2) $I_{pk(s)}$ = secondary peak current.

Graphs valid for discontinuous mode when neglecting secondary diode drop

Fig 27. Waveforms to calculate secondary stroke time

During primary stroke time, the I_{pk} primary increases linear with the slope of the DC voltage over the primary V_{DC} divided by the inductance L_p. The current on the secondary side (I_s) starts with the transformed current to secondary side, $I_{pk(p)} * n$. The decay is linear to zero with a slope of the output voltage V_{OUT} divided by the primary inductance, transferred to secondary side L_p / n^2.

The secondary stroke time t_s can be derived from the secondary current Equation 20, as shown in Equation 21.

$$I_s = n \times I_{pk(p)} - (V_{OUT} (L_p \div (n^2))) \times t \quad (20)$$

The secondary stroke time t_s is reached when $I_s = 0$:

$$t_s = L_p \times I_{pk(p)} \div (n \times V_{OUT}) \quad (21)$$

For correct sampling, the minimum secondary stroke time $t_{s(min)}$ for $I_{pk} = I_{pk(min)} = 1.9$ µs. The ratio between $I_{pk(min)}$ and $I_{pk(max)}$ is 4.9.

When the calculated $t_{s(min)}$ is too short, the time can be increased by lowering nV_{OUT} in the calculation and recalculate the L_p and I_{pk}.

6.3.3 Winding construction

Figure 28 show a suitable set-up of the winding scheme.

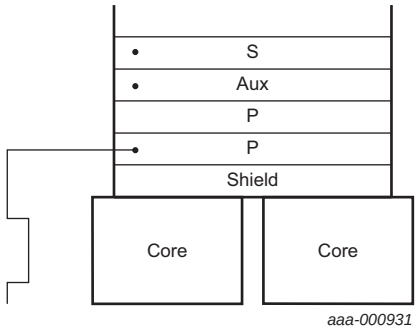


Fig 28. Transformer winding configuration

The first winding called the Shield is a shielding winding that must be one full layer. Connect one side to ground or to the DC voltage side of the main electrolytic capacitor. The primary winding (P) normally needs two or three layers.

The auxiliary winding additional serves as shielding between primary and secondary. For primary sensing, the auxiliary winding needs a tight coupling with the secondary. In this position it also has a good coupling with the primary, leading to more ringing on the auxiliary winding. For optimal performance, the auxiliary winding must be on top of the secondary winding. However, some shielding is needed between the primary and secondary for EMI protection. The TEA172X demo board uses the construction discussed thus far with auxiliary winding between the primary and secondary. This type of construction gives the demo board satisfactory performance.

The secondary winding (S) must be Triple Isolated (TRISO) wire to meet the safety standards.

6.3.4 Safety requirements

As the output power is low, it is possible to use small cores for the transformer, for example, the EE13 and EE16. However, with these transformer sizes, consider the safety requirements for mains isolation. The use of TRISO wire for the secondary winding maintains a small construction size.

Typically the pins of the bobbins for EE13 and EE16 cores are not spaced far enough apart to fulfill the safety distance between hot and cold. Therefore, the solution is to use flying leads to connect the secondary windings far enough from the primary pins at the bobbin. Flying leads are however not convenient for production.

Some bobbins for EE13 and EE16 are designed with the required safety distance by extending the footprint of the secondary side. This type of construction increases the footprint (larger size), but eases production.

6.4 Differences between 11 W and 5 W applications

The following provides a list of differences between the 11 W and 5 W applications. Figure 29 shows the schematic of the 11 W demo board.

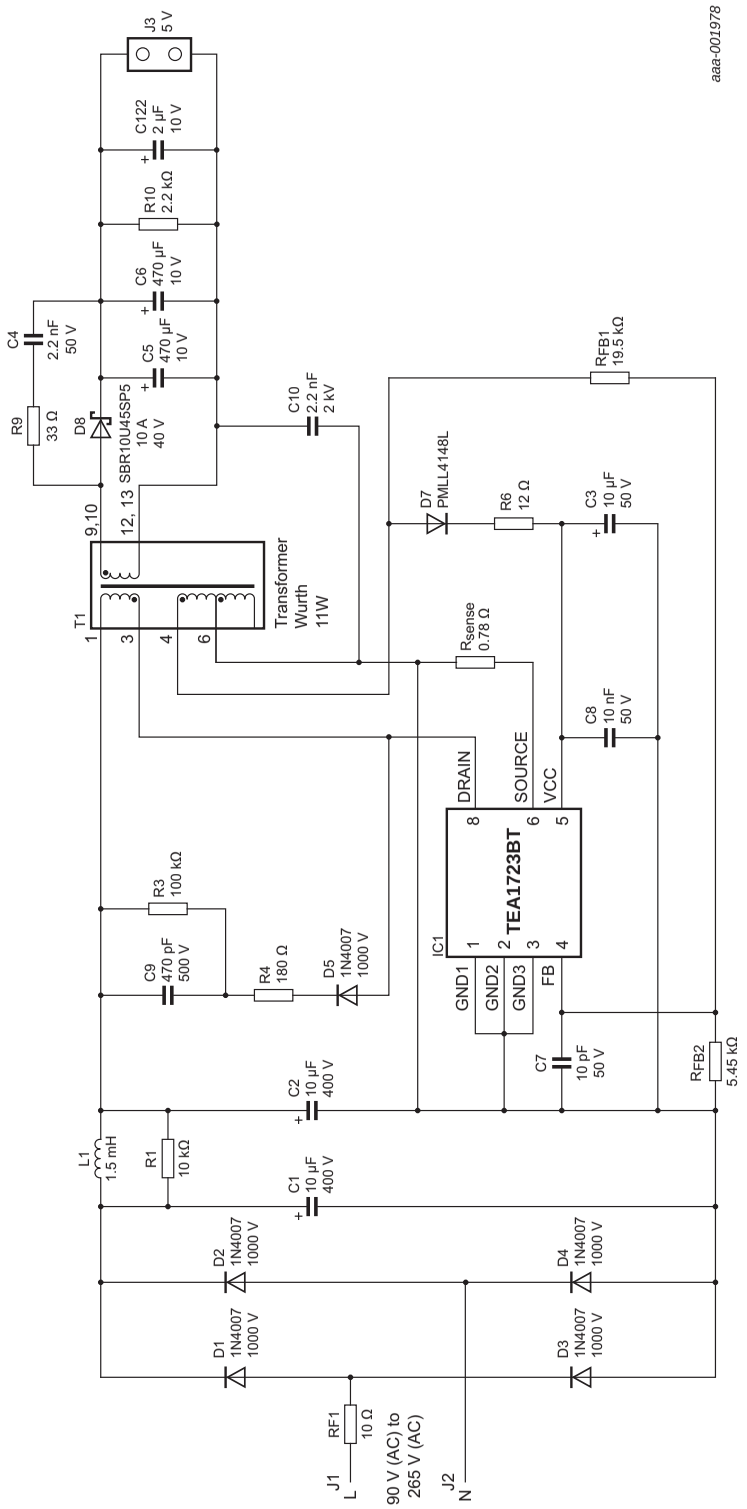


Fig 29. Demo board schematic (11 W)

6.4.1 Input filter and EMI

The configuration for EMI suppression is slightly different. A 2.2 nF Y-cap used over the transformer and the coil in the ground connection of C1 and C2 is replaced by a short-circuit. The EMI suppression is at the limit, to improve the reserve an additional common mode choke before the diode bridge could be added.

6.4.2 Clamp

The values of the components are adapted to match the higher power.

6.4.3 Source resistor

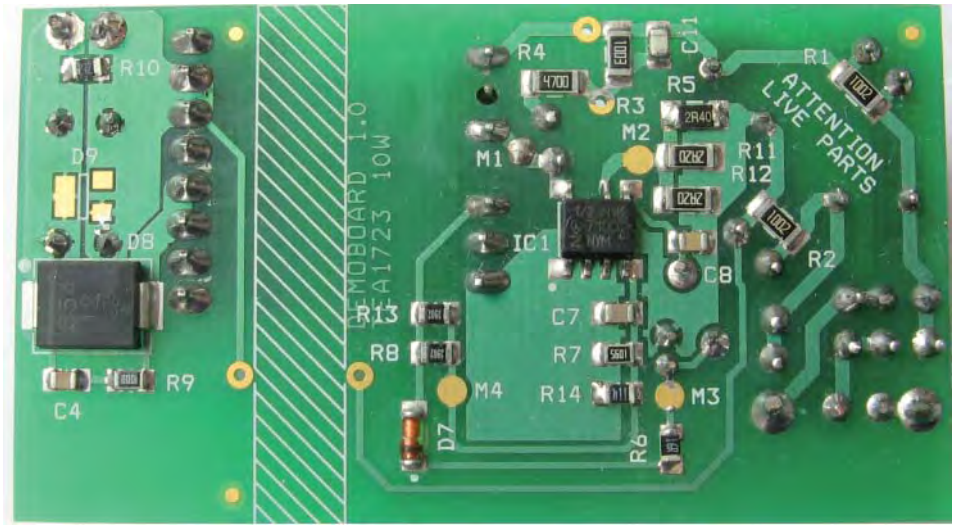
The value of the resistor is adapted to match the higher current.

6.4.4 Secondary side

The value of the output capacitors can remain the same to fulfill the USB 1.1 spec. To reduce the output ripple, a 22 µF ceramic capacitor can be added in parallel to the output capacitors. In addition, the value of the preload resistor is adapted to match the higher no-load power.

6.4.5 Layout considerations

The layout setup for the 11 W version is identical to the 5 W version. Only the cooling is increased to cope with the higher power. The dimension of the copper area is 15 × 10 mm for the 11 W version. The dimension of the copper area for the 5 W version is 8 × 10 mm.



aaa-001989

Fig 30. Demo board layout (11 W)

6.4.6 Calculation L_p and I_{pk}

Figure 31 shows a calculation example for an 11 W application.

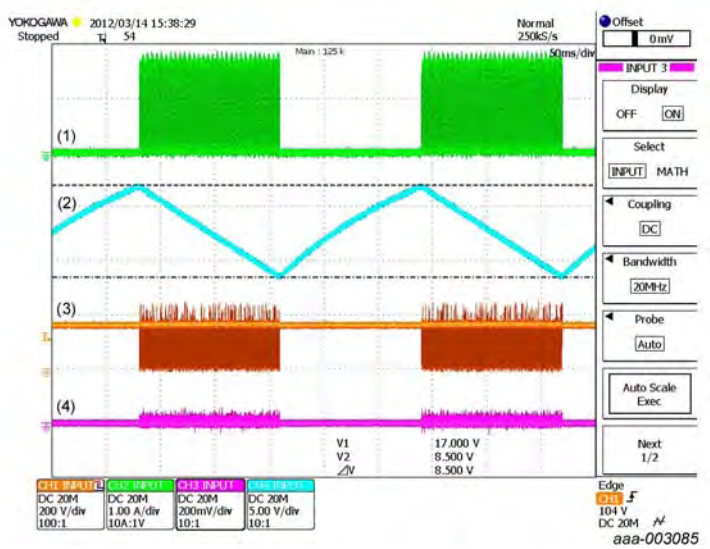
Directions for use	Definition:				
	Physical constants				
	mu_r	1.00			Permeability core
	mu_o	1.26E-06			Permeability vacuum
	ro	1.75E-08			Copper resistance
	ro_increase_per_degree	4.30E-03			For a temperature increase of 100 degrees, the copper resistance increases with 43%
	Values for transformer calculation				
	Isolation thickness triso	1.00E-04	m		Use wire tables, available from manufacturers, e.g. Electrisola
	Isolation thickness lacquer	2.00E-05	m		Use wire tables, available from manufacturers, e.g. Electrisola, use for isolation grade 2
	Input value				
	Calculated				
Fill in the required	**Values, pending on design**				
parameters in the	Vout	5.00	Vdc		Output voltage converter @ max load
green fields	Iout	2.00	A		Maximum output current converter
	Vf	0.60	V		Forward voltage secondary diode
	Cmains	2.00E-05	F		Value total elcap behind rectifier, usual 2 µF per watt output power.
	Vmains_min	85.00	Vac		Lowest specified mains input voltage for full performance
	Fmains	60.00	Hz		Frequency mains voltage @ minimal input voltage
	nVout	72.00	V		Practical value between 60 and 80 Volt, select highest value for which Tsec_min = 1.9 us
The other values are	**Values, fixed by IC design**				
fixed for this design	eff	0.75			Converter efficiency
	Fsw_max	5.20E+04	Hz		Switch frequency at max power
	Tdead_min_perc	0.05			1/Fsw = Tprim + Tsec + Tdead_min, Tdead_min to guarantee discontinuous operation
	Tdead_min	9.62E-07			Tdead_min = 1/Fsw * Tdead_min_perc
	Calculation minimal DC voltage at converter input				
	Pin	13.33	W		Pin = Vout * Iout_max / eff
	Vpeak_elcap	118.81	V		Vpeak_elcap = Vmains_min * SQRT(2) - 2 * drop over bridge diodes (0.7V / diode)
	Vmin_elcap	77.63	V		Vmin_elcap is where the dropping voltage of the elcap meets the rising mains voltage
					For the elcap voltage we can write for Tm, where Tm is the time after reching the Vpeak_elcap:
					0.5 * Cmains * (Vpeak^2 - Velcap^2) = Pin * Tm =>
					Velcap = SQRT((Vpeak^2) - ((Pin * Tm)/(0.5 * Cmains)))
					For the rising voltage of the mains the formula is:
					Vmains = Vpeak * sin (2*pi*Fmains*(Tm - 1/(4*Fmains)))
	Calculation Ipk, Lp				
					Derivation:
				1	Pin = Fsw_max * 0.5 * Lp * Ipk^2
				2	Pin = Pout/eff.
				3	Ipk = Vmin_elcap * Tprim / Lp
				4	Ipk = nVout * Tsec / Lp
				5	Tprim + Tsec + Tdead_min = 1/Fsw_max
					Substitute 3 and 4 in 5
					(Lp*Ipk)/Vmin_elcap + (Lp*Ipk)/nVout + Tdead_min = 1/Fsw_max
					Lp*Ipk = (1/Fsw_max - Tdead_min)(1/(1/Vmin_elcap + 1/nVout) = (1/Fsw_max)(1-Tdead_min_perc)(1/(1/Vmin_elcap + 1/nVout)
					Substitute Lp*Ip in 1
	Ipk	7.51E-01	A		Ipk = (2 * Pin * (Vmin_elcap + nVout)) / ((Vmin_elcap * nVout) * (1-Tdead_min_perc))
	Lp	9.08E-04	H		Lp = (1/Fsw_max - Tdead_min) * 1 / (1/Vmin_elcap + 1/nVout) * 1/Ipk
	Tsec_max	9.48E-06			Tsec = Lp * Ipk / (nVout)
	Tsec_min	1.93E-06			Tsec_min = Tsec_max * (Ipk_min/Ipk_max) = Tsec_max / 4.9

aaa-002013

Fig 31. L_p and I_{pk} calculations (11 W)

6.5 Short-circuit behavior

The TEA172x can handle a short-circuit on the secondary side in a safe way. In Figure 32 the relevant signals are given during a short.



(1) I_{OUT} in short-circuit condition.

(2) V_{CC}.

(3) V_{DRAIN}.

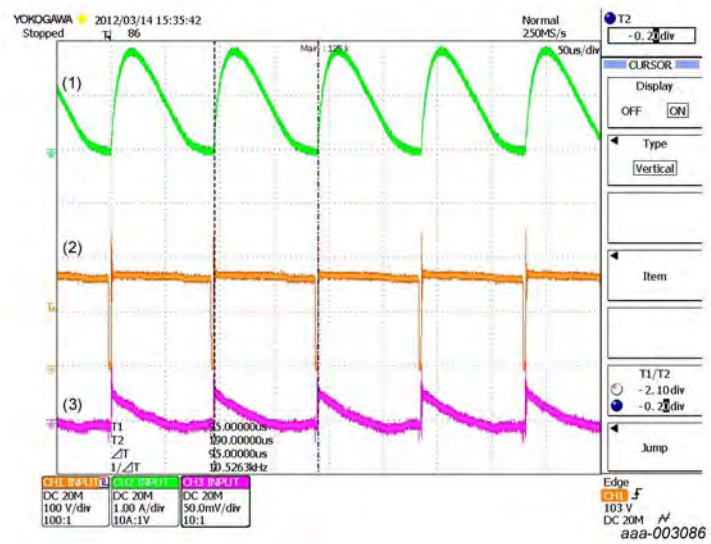
(4) V_{OUT}.

Fig 32. Signals during a short circuit of V_{OUT}

When the output is short circuited, the TEA172x runs in current mode.

The voltage on the auxiliary winding is related to the V_{OUT} trigger level which is less than 8.5 V. The VCC capacitor is no longer charged. When the VCC supply < $V_{CC(stop)}$ trigger level (8.5 V), switching stops. The high-voltage current source is enabled and charges the capacitor connected to pin on VCC. When the VCC voltage > 17 V ($V_{CC(startup)}$), switching is started and the circuit delivers current to the short-circuit. Switching continues until the VCC supply < $V_{CC(stop)}$ trigger level (8.5 V) causing the sequence to repeat.

Looking in more detail at the waveforms, the TEA172x triggers demagnetization protection when the output is short circuited (See Figure 33).



(1) I_{OUT} in short-circuit condition.

(2) V_{DRAIN}.

(3) V_{OUT}.

Fig 33. Detailed waveforms while switching during a short circuit

After building up energy during primary stroke, the energy is delivered to the secondary diode and the short circuited output. The demagnetization requirement (V_{FB} < 50 mV) is only valid when all energy is delivered to secondary side. Once this occurs, switching is released. The demagnetization protection now determines the switching frequency ensuring the energy delivered during the short-circuit is limited.

The primary power, taken during the hiccup mode with V_{OUT} short circuited, is measured for the TEA172x application boards as given in Table 5.

Table 5. Input power with V_{OUT} short circuited

The TEA1721XT are 5 W versions and the TEA1723XT are 11 W versions.

AC V_{IN} RMS (V)	TEA1721XT (W)	TEA1723XT (W)
90	0.26	0.42
115	0.29	0.45
230	0.39	0.59
265	0.43	0.62

The primary power is low enough for the circuit to survive a short-circuit for an indefinite time

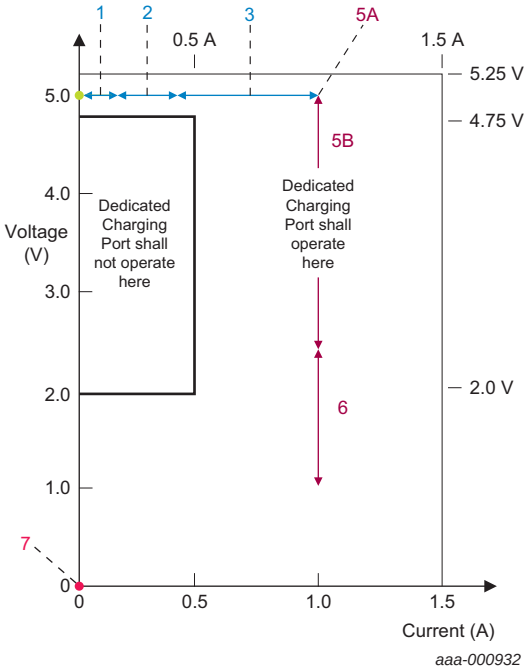
7. Appendix

7.1 USB specification

The TEA172X is designed to fulfill the USB specification for chargers. Currently, USB 1.1 is used, however USB 1.2 is advancing. The most important requirements are as follows.

7.1.1 USB 1.1

Figure 34 shows a graph of the static voltage versus current requirement for a USB 1.1 charger.



(1) CVB: Burst mode with energy saving: no-load 10 mW to low load of 120 mW.
(2) CVC: 120 mW up to 2 W.
(3) CVF: 2 W up to 5 W.
(4) CP: 5 W with transition from CV to CC.
(5) CCF: 5 W down to 2.5 W
(6) CCC: Constant voltage with burst mode. 2.5 down to 1 W
(7) Start-up and UVLO. No power conversion.

Generally, the graph is valid for a quasi-stationary load and is without jitter and without spread.

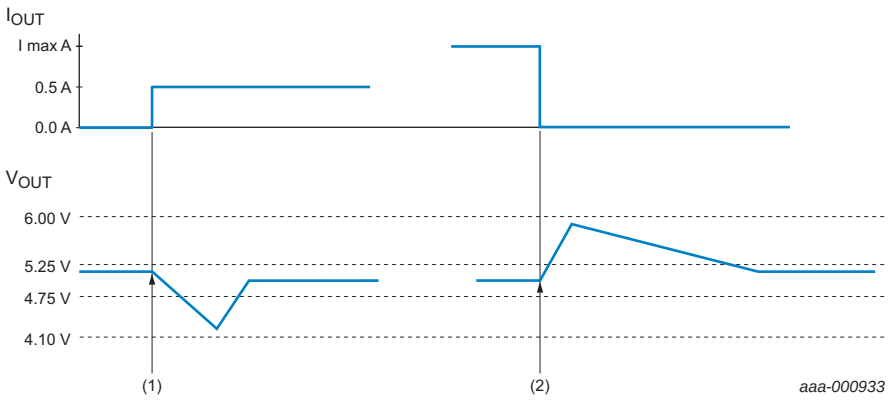
Fig 34. USB 1.1 static behavior and TEA172X operation modes

Figure 34 shows the voltage versus current for a 5 W USB charger using the TEA1721. The USB 1.1 specification requires precise voltage regulation (5 V ± 5 % or 4.75 V - 5.25 V) up to 0.5 A. Higher than 0.5 A, the requirement is that the output current remains between 0.5 A and 1.5 A. The output voltage must remain lower than 5.25 V.

If V_{OUT} drops below 2 V, the power supply is allowed to shut down, that is, it starts to “Hiccup”. Alternatively, the power supply can continue to deliver current for as long as the output current remains lower than 1.5 A. The characteristic of most chargers is to maintain the output voltage between 4.75 V and 5.25 V until maximum output power is reached. Thereafter, switch to current mode for charging.

Current mode has to work at least until an output voltage of 2 V. Lower than 2 V, behavior is not critical unless the output current increases higher than 1.5 A. For the USB 1.1 characteristic the different operating modes of the TEA172X are indicated.

Figure 35 shows the dynamic behavior requirements of USB 1.1.



(1) Load step 0 A => 0.5 A. Requirements:
- V_{OUT} must remain above 4.1 V
- V_{OUT} average (over 1 s) must remain between 4.75 V and 5.25 V

No time limits for recovery

(2) Load step I_{max} A => 0 A. Requirement:
- V_{OUT} must remain below 6 V
- V_{OUT} average (over 1 s) must remain between 4.75 V and 5.25 V

No time limit for recovery

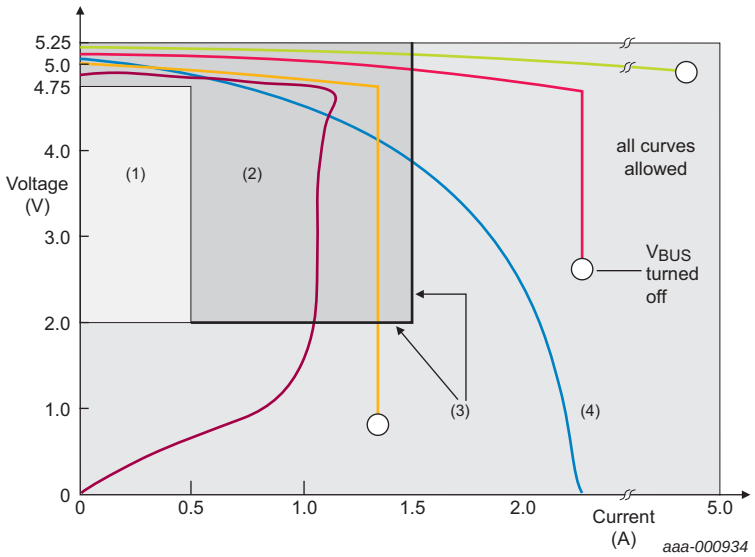
Fig 35. USB 1.1 dynamic behavior

For any load step between 0 A and 0.5 A, V_{OUT} is not allowed to drop below 4.1 V. This requirement is used to calculate the size of the output capacitors, see Section 5.6.

For any load step between $I_{OUT(max)}$ and 0 A, the output voltage must not rise higher than 6 V. The output voltage must remain between 4.75 V and 5.25 V when averaged over 1 second.

7.1.2 USB 1.2

Figure 36 shows the static behavior for USB 1.2, which is less demanding on a number of aspects compared to USB 1.1.



(1) Charging port operation not allowed

(2) Required operating range for Dedicated Charging Port (DCP)

(3) Valid load curve must cross either line

(4) Continuous current regulation allowed. Current limit trip operation allowed.

Generally, the specification for the output voltage remains narrow until an output current of 0.5 A (4.75 V to 5.25 V). No requirement for current limitation or minimal required V_{OUT} (V_{BUS}).

Fig 36. USB 1.2 static behavior

The USB 1.2 specification is identical to USB 1.1 up to an output current of 0.5 A. At 0.5 A, V_{OUT} must remain between 4.75 V and 5.25 V. Above 0.5 A, there are no requirements except that the output voltage must remain below 5.25 V and the output current must remain below 5 A.

At output currents <1.5 A, the device must operate until the output voltage is 2 V. Below an output voltage of 2 V or out put current of 1.5 A, the device can shut down, “Hiccup” or deliver any current below 5 A. In practice, most customers do not allow currents in this mode above the nominal charge current to avoid excessive dissipation.

A major relaxation of USB 1.2 related to dynamic behavior are load steps. Load steps have been divided into two ranges and three current levels. See Table 6

Table 6. Load steps

I_{DCP}	Min	Max	Unit
Low	0	0.03	A
Mid	0.03	0.1	A
High	0.5	-	A

Load steps are divided into the three Dedicated Charging Port (DCP) current ranges:

- I_{DCP} Low => I_{DCP} Mid
- I_{DCP} Mid => I_{DCP} High
- I_{DCP} Low => I_{DCP} High

The additional I_{DCP} Mid level allows for relaxation of the undershoot requirements for primary sensed chargers with low standby power, provided the USB device is designed for USB 1.2. The requirements for undershoot during current steps from Low to Mid and Mid to High are as shown in Figure 37:

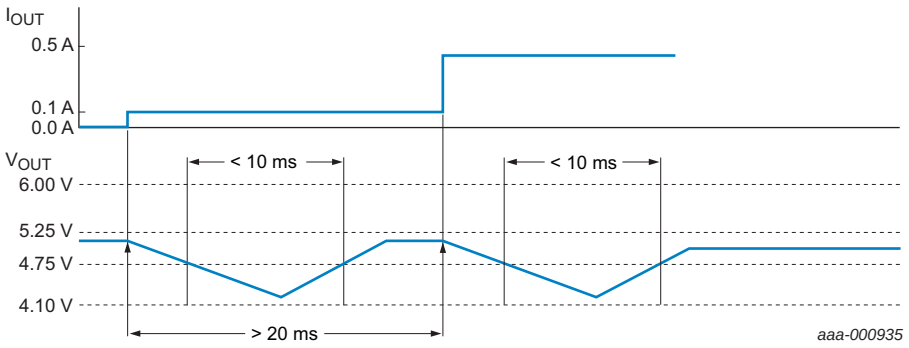


Fig 37. USB dynamic undershoot 1

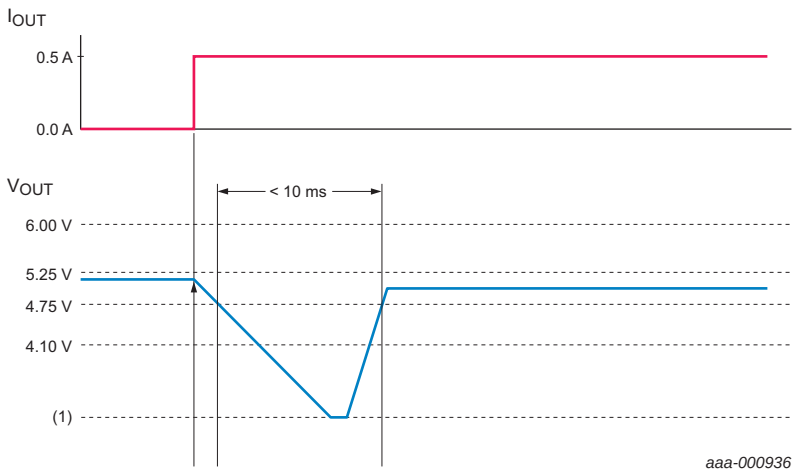
For load steps between:

- I_{DCP} Low => I_{DCP} Mid (0 A => 0.03 A to 0.10 A) and I_{DCP} Mid => I_{DCP} High (0.03 A to 0.10 A => 0.5 A)

the following applies:

- V_{OUT} must remain above 4.1 V
- Duration undershoot V_{OUT} < 4.75 V must be < 10 ms
- Minimum time between load step 0 A => 0.03 A to 0.10 A and 0.03 A to 0.10 A => 0.5 A is 20 ms.

The requirements for undershoot during a current step from Low to High are as shown in Figure 38



(1) Load voltage attached PD (USB PD)

Fig 38. USB dynamic undershoot 2

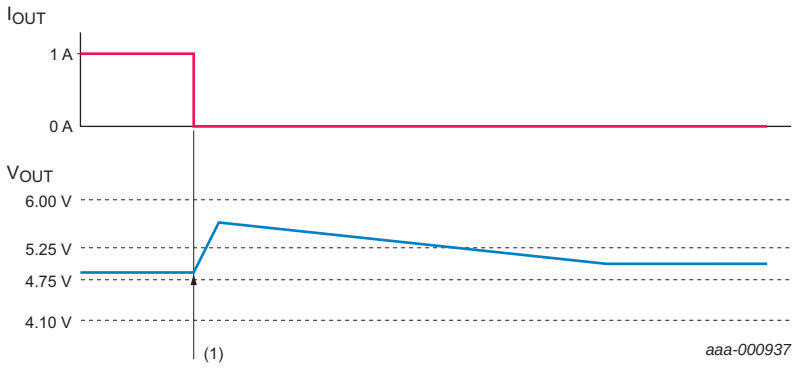
For any load step between:

- I_{DCP} Low => High (0 A to 0.03 A => 0.5 A)

the following applies:

- V_{OUT} can drop to the battery voltage of the attached Portable Device (PD)
- Undershoot (V_{OUT} < 4.75 V) must be < 10 ms

The requirement for load steps from high to low is the same as for USB 1.1. See Figure 39



(1) Load step 1 A => 0 A (or any other load step down). Requirement, V_{OUT} must not exceed 6 V.

Fig 39. USB 1.2 dynamic overshoot

In general, the output voltage must not rise above 6 V for any load step, during switch-on or during switch-off.

8. Abbreviations

Table 7. Abbreviations

Acronym	Description
CC	Constant Current
CCC	Constant Current with Current mode
CCF	Constant Current with Frequency mode
CP	Constant Power
CVB	Constant Current with Burst mode
CVC	Constant Voltage with Current mode
CVF	Constant Voltage with Frequency mode
CV	Constant Voltage
DCP	Dedicated Charging Port
EMI	ElectroMagnetic Interference
ESR	Equivalent Series Resistance
HVAC	Heating, Ventilating and Air Conditioning
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
OVP	OverVoltage Protection
PD	Portable Device
UVLO	UnderVoltage Lockout
UVP	UnderVoltage Protection

9. References

[1] **TEA1721AT\BT\DT\FT —** data sheets: Ultra-low standby SMPS controller with integrated power switch

[2] **TEA1723AT/BT/DT/FT —** data sheets: Ultra-low standby SMPS controller with integrated power switch data sheet

[3] **UM10520 —** TEA1721 Isolated 3-phase universal mains flyback converter demo board user manual

[4] **UM10521 —** TEA1721 isolated universal mains flyback converter demo board user manual

[5] **UM10522 —** TEA1721 non-isolated universal mains buck and buck/boost converter demo board user manual

[6] **UM10523 —** TEA1721 universal mains white goods flyback SMPS demo board user manual

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Date of release: 1 May 2012
Document identifier: AN11060